Atoms to go…

Ionic memory and data storage

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adesto TECHNOLOGIES

- No exponential is forever…
- The need for new memory
- The contender - resistive memory
- Introduction to ionic memory
- Device characteristics and models
- Materials at the nanoscale
- Active and passive arrays
- Real stuff
- Questions and discussion

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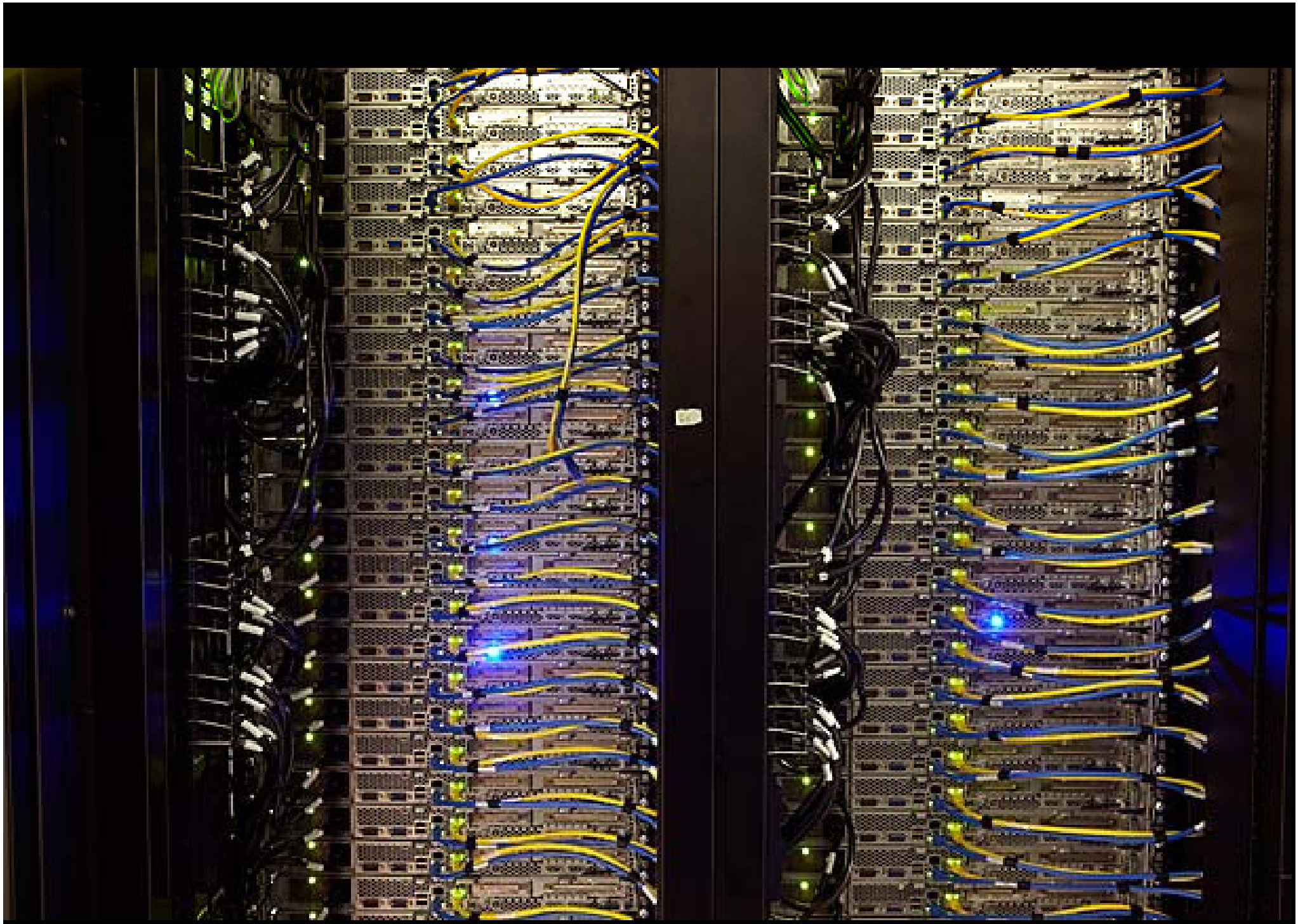
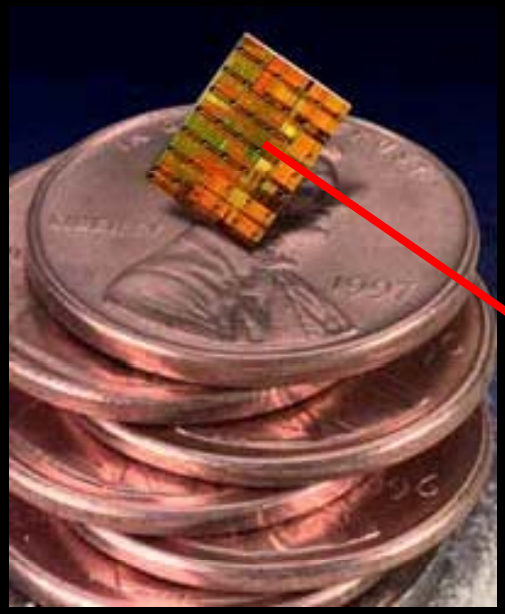
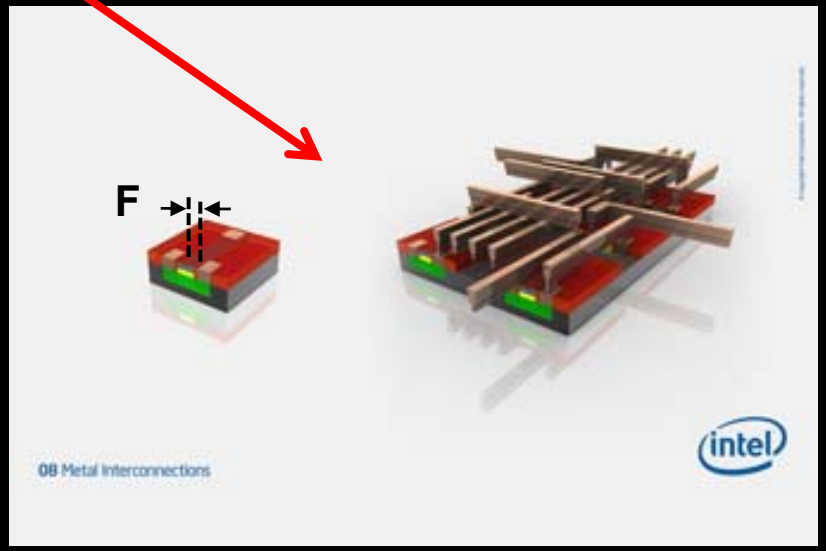
“The future ain't what it used to be.” - Yogi Berra



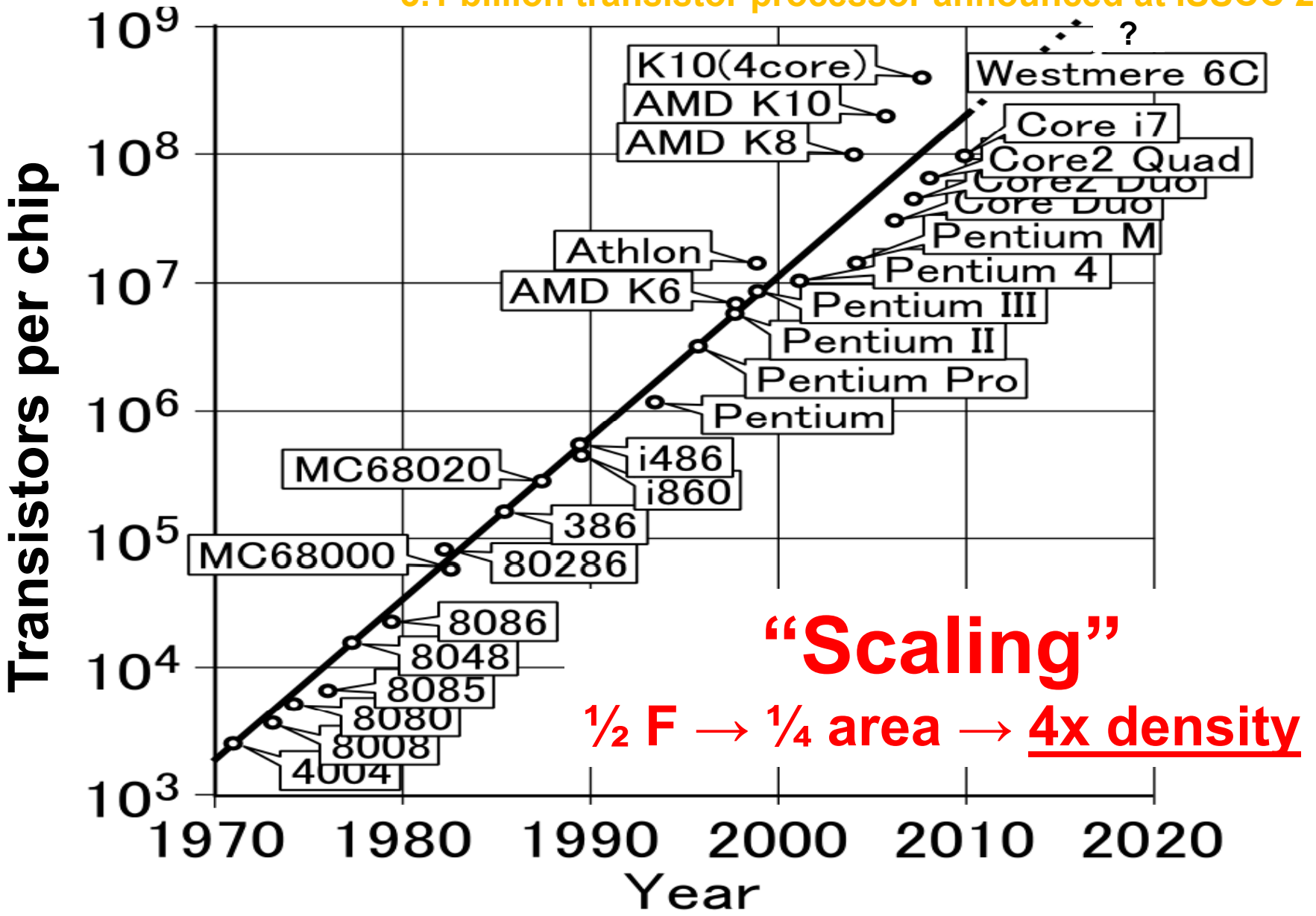
Facebook server racks – www.time.com




F
08 Metal Interconnections
intel

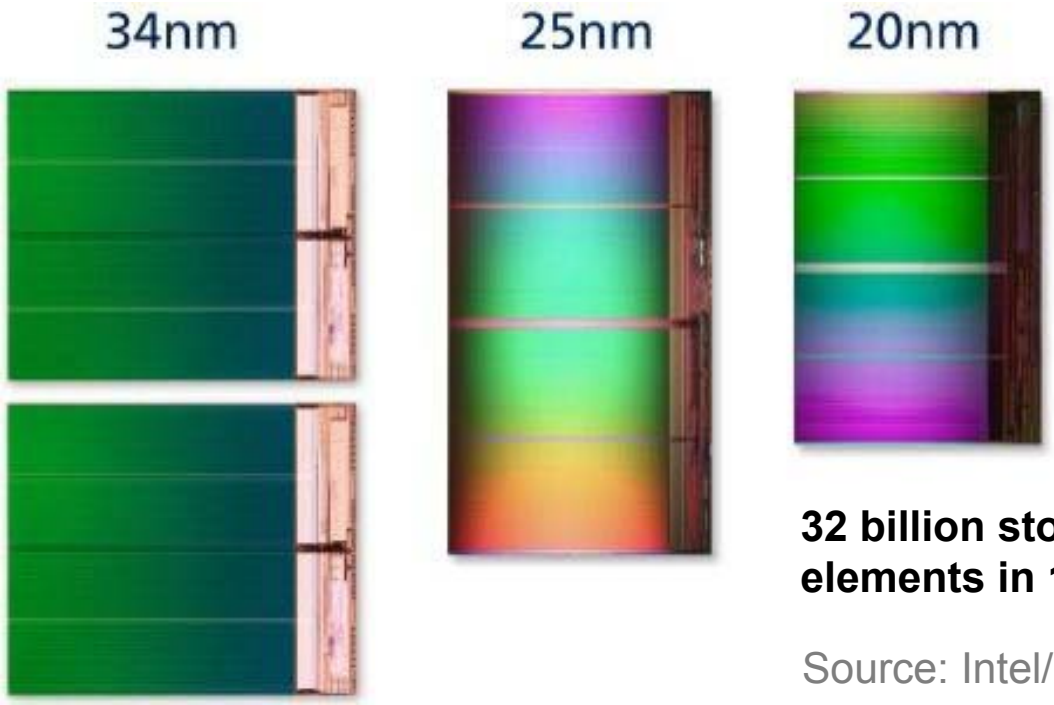
Exponential growth - Moore's Law

3.1 billion transistor processor announced at ISSCC 2011



http://commons.wikimedia.org/wiki/File:Moores_law_(1970-2010).PNG

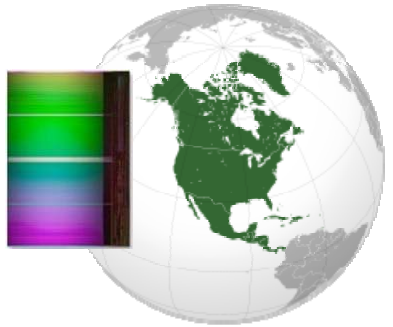
64 Gb Flash memory shrink



32 billion storage elements in 118 mm^2

Source: Intel/Micron

If a 20 nm feature in the chip was the size of a residential street, how big would the chip be?

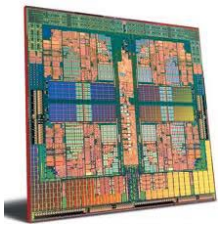


Why the future ain't what it used to be

- **The fruits of Moore's "Law"**
  - **Discrete electronics turned into microelectronics and Moore's *Observation* was born**
  - **More devices/cm^2 means more performance for less $$**
    - » **Higher speed, higher reliability, smaller systems also result**
  - **The best way to get more devices per cm^2 is to make them smaller – the cult of *scaling* was established**
- **But scaling is breaking down at nano-dimensions**
  - **Nano devices don't behave like wee versions of their bigger brothers**
    - » **Inhomogeneity and quantum mechanics make life interesting**
  - **Tightly packed structures, ultra-thin layers, small numbers of electrons all lead to big issues**

The end of scaling as we know it?

- **"…innovation has overtaken scaling as the driver of semiconductor technology performance…" - Bernard Meyerson, IBM**
- **Really smart design will keep logic on the Moore's Law performance trajectory**
  - **e.g., multi-core processors…**



- **But what about memory?**

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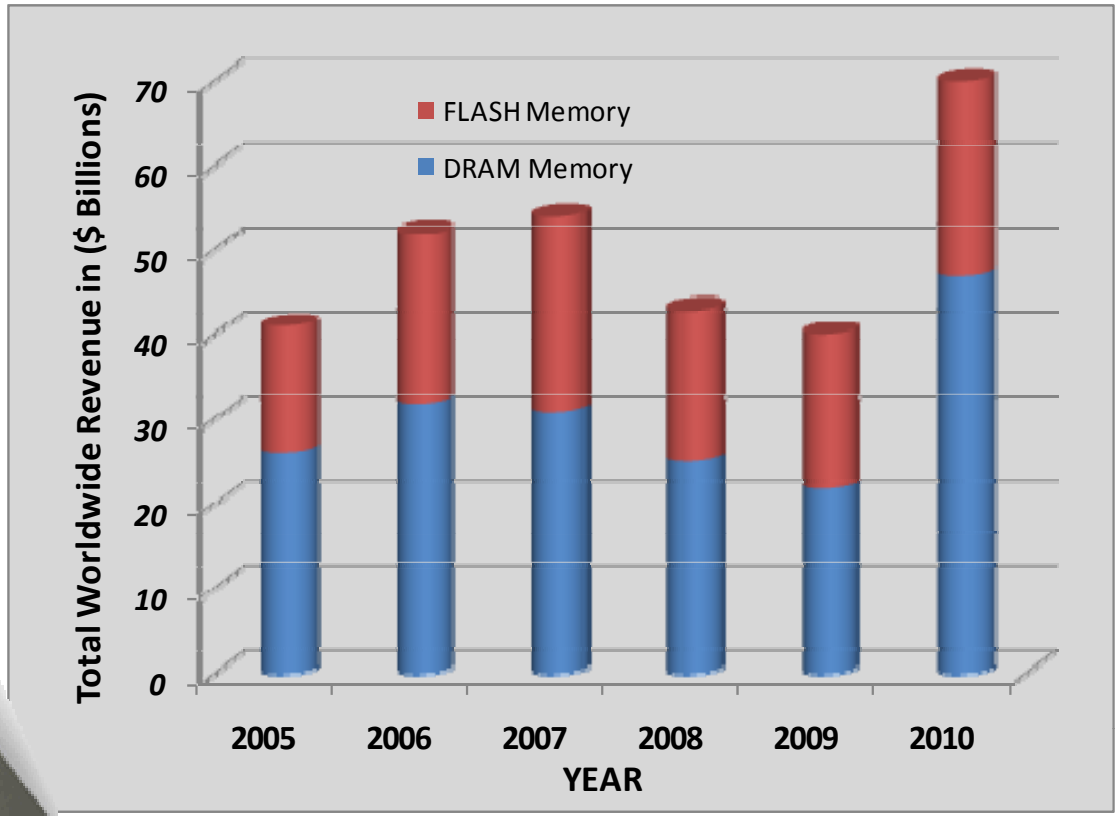
The memory market

Markets and applications utilizing memory devices:

Computers
Cell Phones
Music Players
Digital Cameras
Appliances
Cars/automotive
Printers
TVs
Game consoles
Video players
Servers

Solid state drives (SSDs)

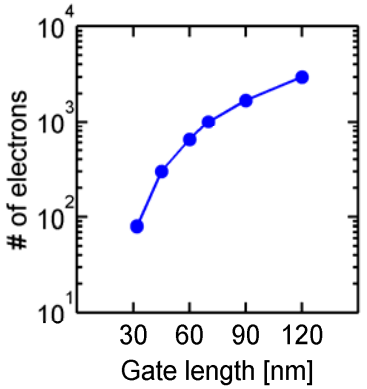
Total memory market size for two key types of memory: *Flash* and *DRAM*



Source: Denali, 2010

The challenge we are facing…

- The demand for memory capacity is growing
  - » You can never have too much memory!
- Memory scaling is stalling as existing charge-storage devices will struggle to meet future industry requirements
  - » Smaller devices mean fewer electrons stored
    - small charge is difficult to retain and detect
  - » Lower programming voltage is required to prevent closely-spaced devices talking to one another
    - programming time rises greatly
    - compensate by changing structure
    - results in greatly reduced retention



Flash storage cell in a Samsung 4 Gb MLC chip taken from an iPod Nano by ChipWorks

Requirements for next-generation memory

- **Physical scalability**
  - **Assume 10^{12} bits in a "chip-like" form factor with extremely compact periphery/high array efficiency**
  - **For a 20 x 20 mm^2 terabit array area and a 4 - $6F^2$ cell, F must be less than 10 nm**
  - **Not good news as nobody knows how to define/make reliable sub-10 nm metallic interconnects in a manufacturing environment!**
  - **Implies F should be > 10 nm but then multi-level cell and/or multi-layer array is absolutely necessary to achieve density**

More requirements…

- **Electrical scalability**
  - **At the F = 22 nm technology node, the supply voltage is < 1V**
  - **Critical current at 22 nm is no more than a few tens of μA**
  - **Programming in the pJ range for energy conservation and heat dissipation**
- **Manufacturability /economics**
  - **Overall cost and *cost of first bit***
  - **Compatible with existing processes**
  - **Longevity (multiple applications and technology generations)**
  - **Reliability… the killer of promising new technologies!**

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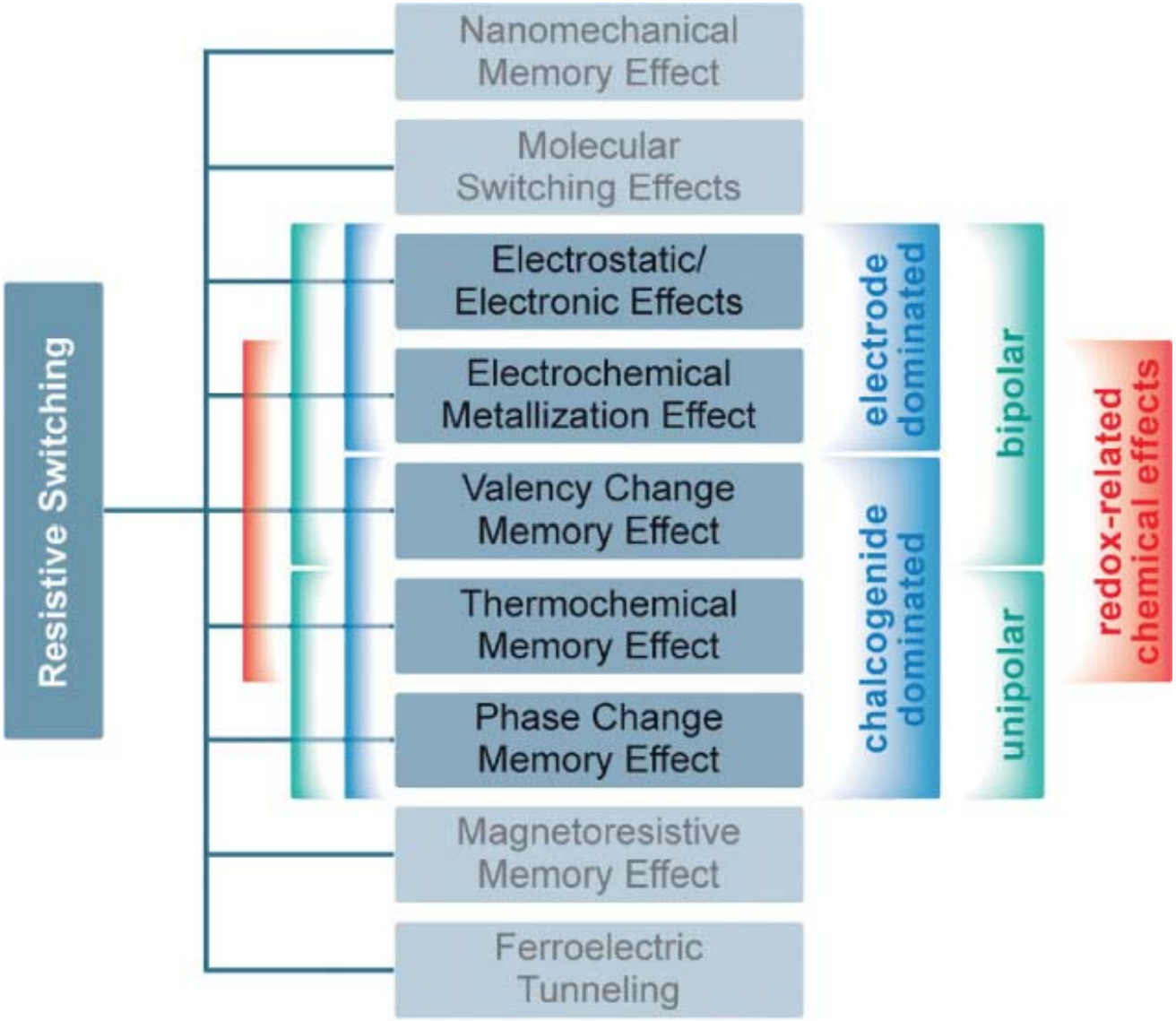
The basics of resistive memory

- **Change in resistance on the application of a voltage/current**
  - **Devices have a high resistance state (*HRS, reset, off*) and one *or more* low resistance states (*LRS, set, on*)**
  - **Usually not a subtle effect**
- **A variety of mechanisms are possible**
  - **Field- or current-driven**
  - **Can involve a *change in material***
  - **Bulk, interfacial, or *filamentary***
- **Can be *unipolar* or *bipolar***

Resistive memory taxonomy



R. Waser et al., "Redox-Based Resistive Switching Memories – Nanoionic Mechanisms, Prospects, and Challenges", Adv. Mater., vol. 21, 2632–2663 (2009).

Physical changes in materials

- **“Heine Rohrer showed five examples of where, if the space becomes small, new phenomena happen… if the distance is very short, diffusion, atomic or ionic motion, is very fast.”**

  Interview with Masakazu Aono, ACS Nano, Vol. 1, No. 5, 379-383 (2007)

- **Physical changes can result in highly stable, widely spaced states**
  - **inherently non-volatile resistance levels**
  - **small # of atoms can lead to large macroscopic effects**
- **Filamentary processes are typically more scalable as on-state resistance is independent of device area**
  - **filaments can be a few nm in radius**

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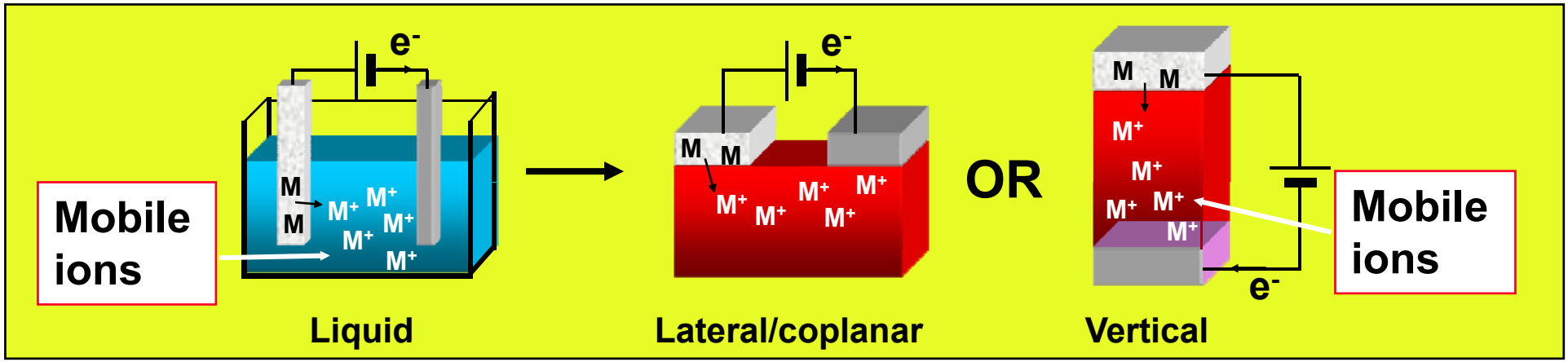
Solid electrolytes

- ***Solid electrolytes*** **behave like liquid electrolytes…**

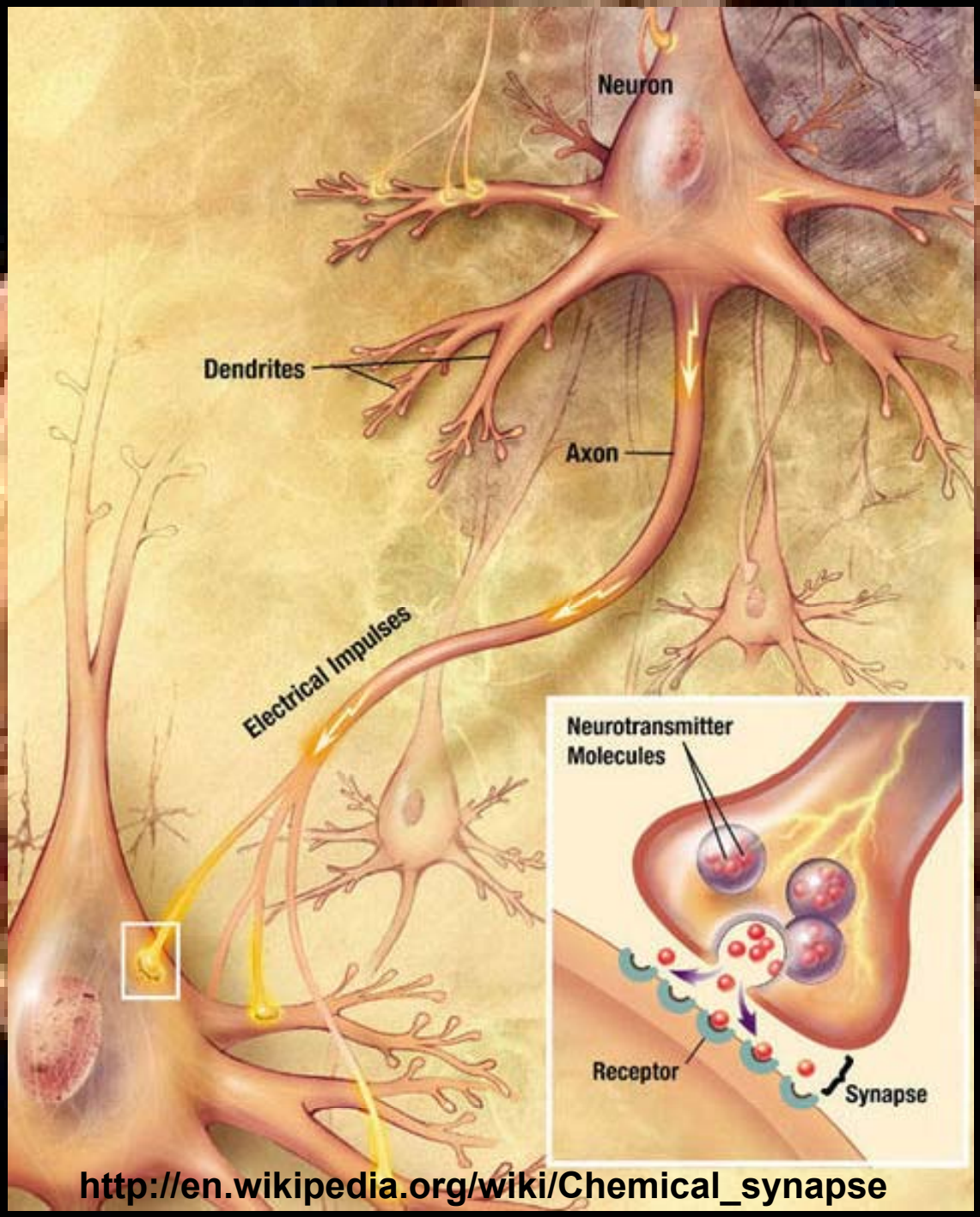


- **Ions move under the influence of an electric field and *electrochemical reactions* are possible**

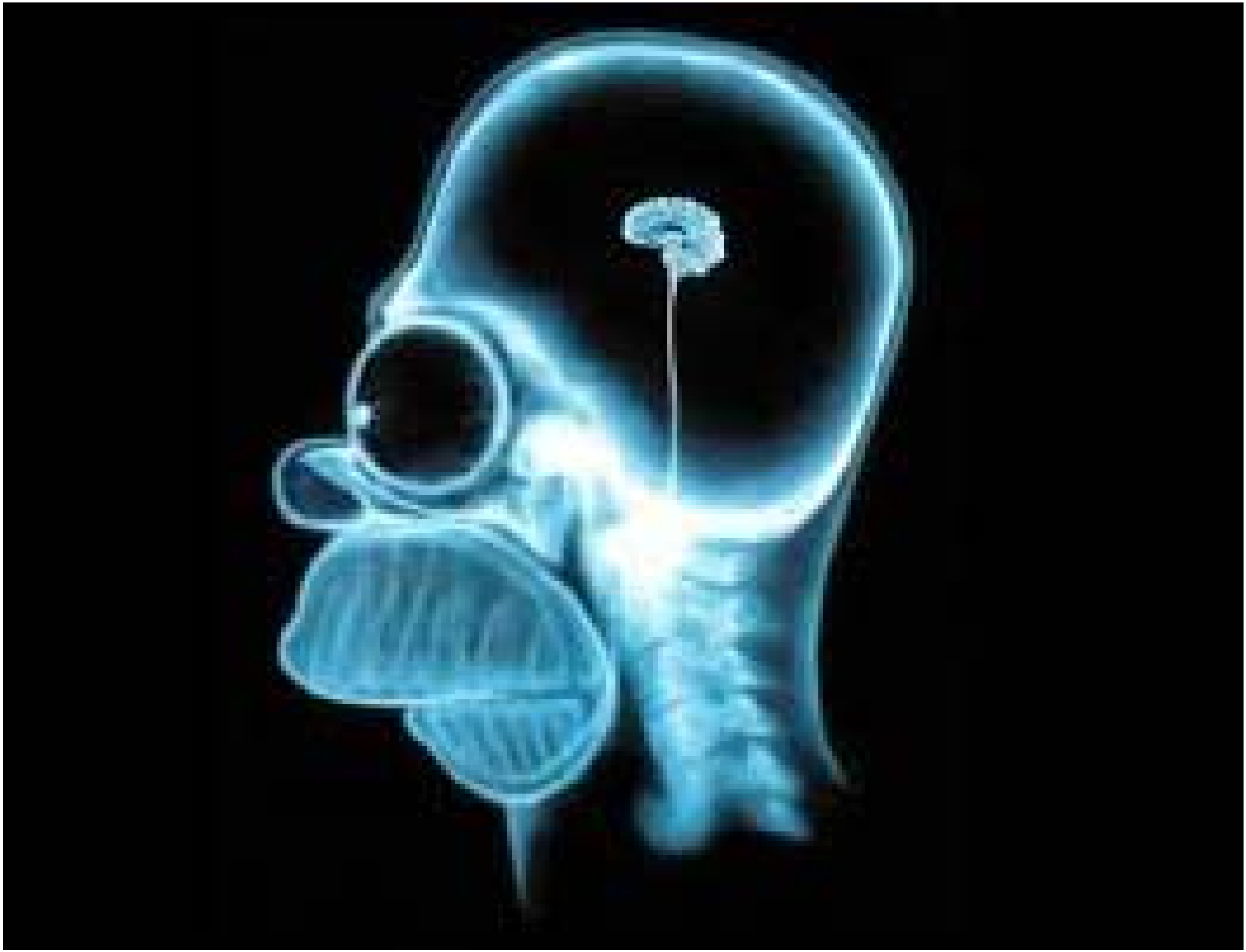
cathode (conductor): $M^+ + e^- \rightarrow M$ *reduction*

anode (with excess M): $M \rightarrow M^+ + e^-$ *oxidation*

Electrochemistry occurs at a *few 100 mV*



http://en.wikipedia.org/wiki/Chemical_synapse



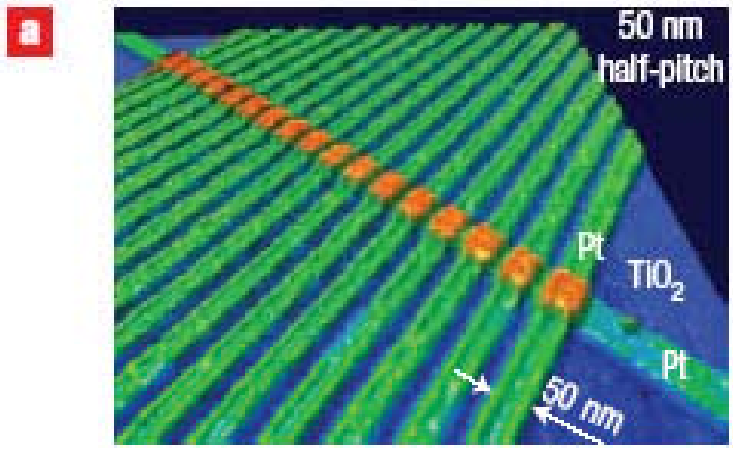
Nanoionics-based resistive switching memories

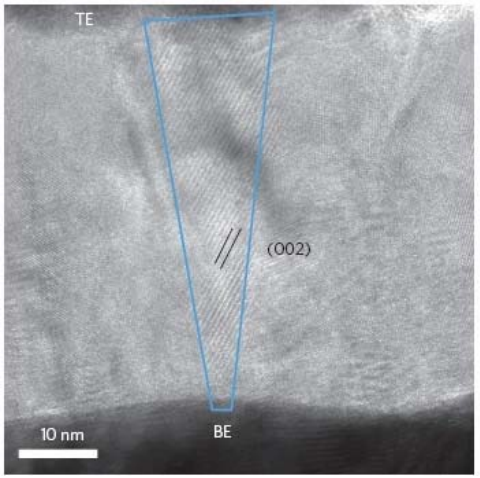
Rainer Waser and Masakazu Aono

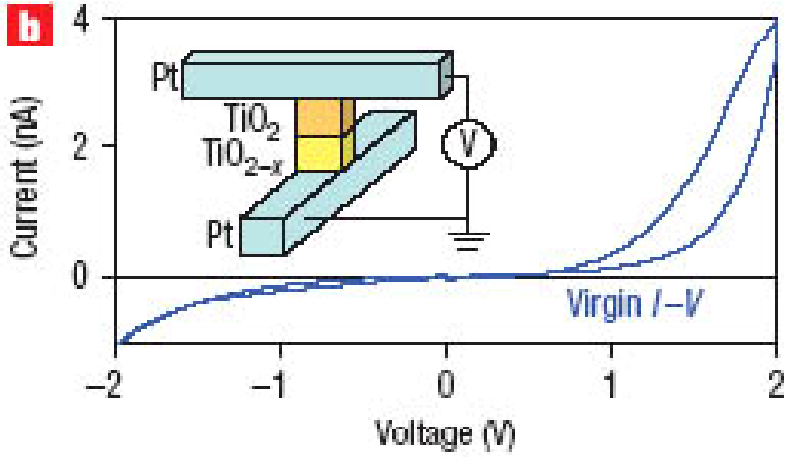
nature materials | VOL 6 | NOVEMBER 2007 | www.nature.com/naturematerials

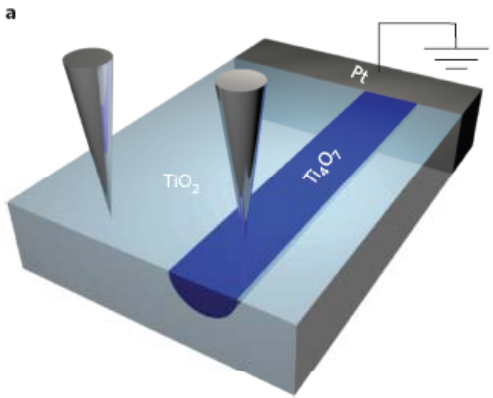
…**ion-migration** effects are coupled to **redox processes** which cause the **change in resistance**. They are subdivided into **cation-migration** cells, based on the electrochemical **growth and dissolution of metallic filaments**, and **anion-migration** cells, typically realized with transition metal oxides as the insulator, in which **electronically conducting paths of sub-oxides are formed and removed**…

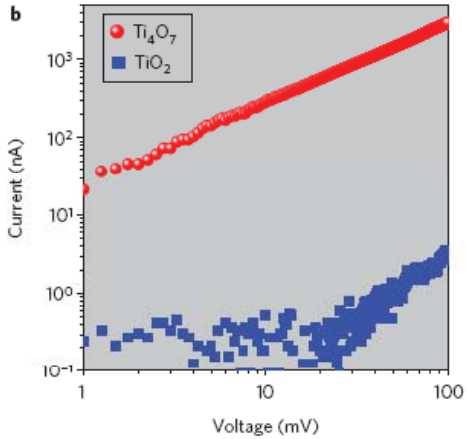
The famous Memristor









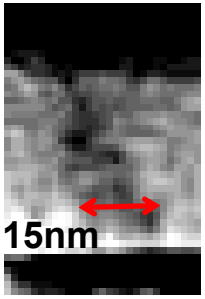


J. J. Yang, M. D. Pickett, X. Li, D. A. A. Ohlberg, D. R. Stewart, R. S. Williams, "Memristive switching mechanism for metal/oxide/metal nanodevices," Nature Nanotechnology, Vol. 3, 429 (2008).

D.-H. Kwon *et al.*, "Atomic structure of conducting nanofilaments in TiO_2 resistive switching memory," Nature Nanotechnology, published online: 17 January 2010, DOI: 10.1038/NNANO.2009.456(2010).

Cation-based solid electrolyte device

Cryo-TEM image of filament



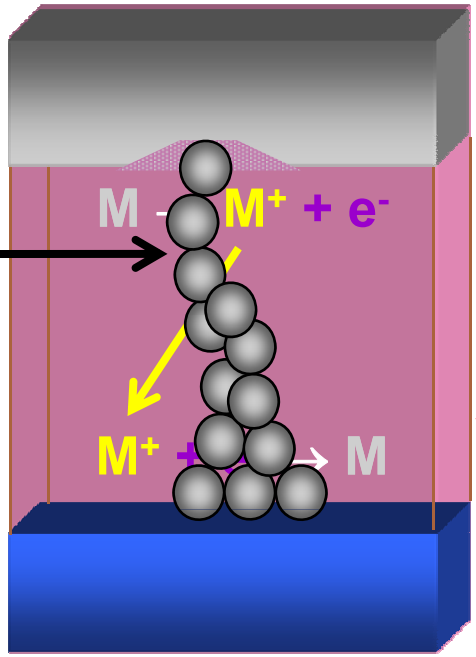
Metallic electrodeposit

low resistance

Glassy electrolyte

high resistance

Mobile ions added during processing or via *electroforming*



e⁻ +

Oxidizable electrode

Ion current

Bias > write threshold

Inert electrode

e⁻ −

Low energy approach

High energy approach

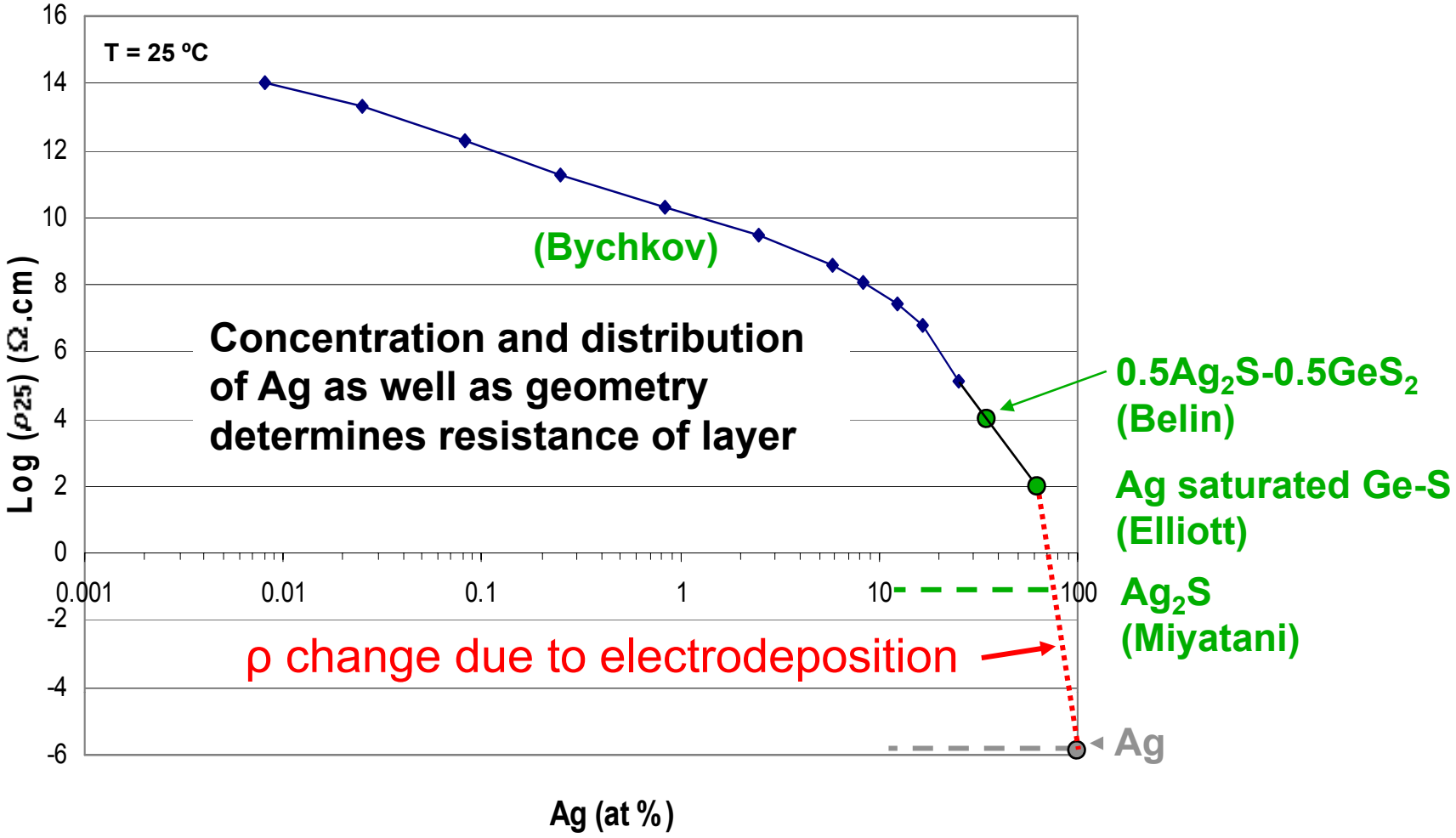
Reverse bias or high forward current dissolves electrodeposit

Materials - electrolytes & electrodes

Electrolyte	Electrode metals	
	Ag	Cu
Ge_xS_y	*W*	*W*
Ge_xSe_y	*W, Pt, Ni*	*W*
Ge-Te	*TiW*	*TaN*
GST	*Mo*	
As-S	*Au*	
$Zn_xCd_{1-x}S$	*Pt*	
Cu_2S		*Pt, Ti*
Ta_2O_5		*Pt, Ru*
SiO_2	*Co*	*W, Pt, Ir*
WO_3	*W*	*W*
TiO_2	*Pt*	
ZrO_2	*Au*	
MSQ (SiO_2)	*Pt*	
CuTe/GdOx		*W*
Ge_xSe_y/SiO_x		*Pt*
Ge_xSe_y/Ta_2O_5		*W*
Cu_xS/Cu_xO		*Pt*
Cu_xS/SiO_2		*Pt*

Compiled by John Jameson, Adesto Technologies

Electrolyte example: Resistivity of Ge-S vs. Ag content

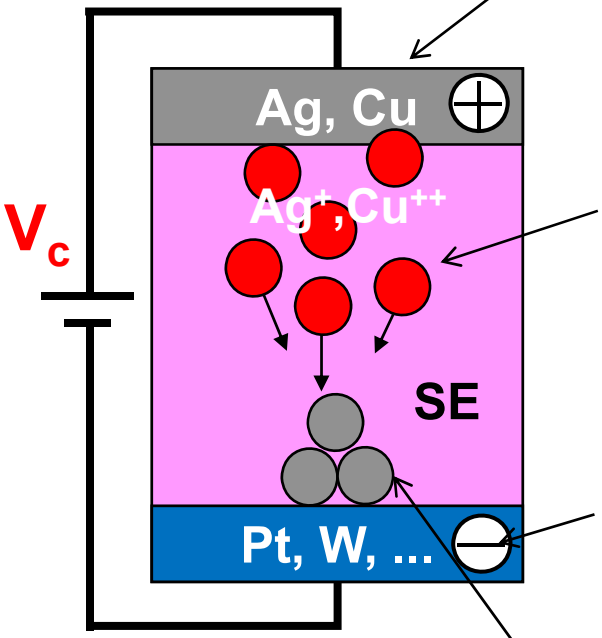


Growth of electrodeposit

Reversal of electrodeposit growth

Reaction environment

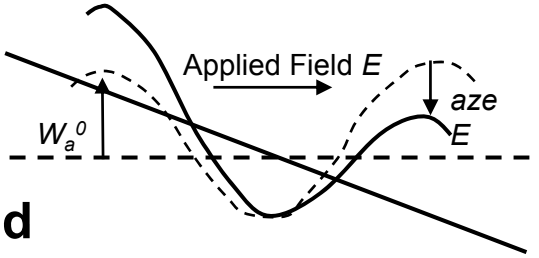
$j \sim \exp(qV_c/kT)$



Anodic dissolution

- equilibrium → oxidation for applied bias
- electrochemical electron transfer (Butler-Volmer)
- no overpotential, fast reaction

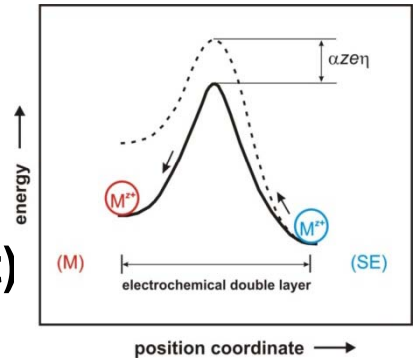
Cation transport



- drift /diffusion transport
- high fields → drift dominant
- non-linear, very fast at high field

Cathodic deposition

- electrochemical electron transfer (Butler-Volmer)
- crystallization overpotential



Filament growth

- Even with multiple nucleation sites, "winner takes all" (field confinement)
- Filament forms within electrolyte

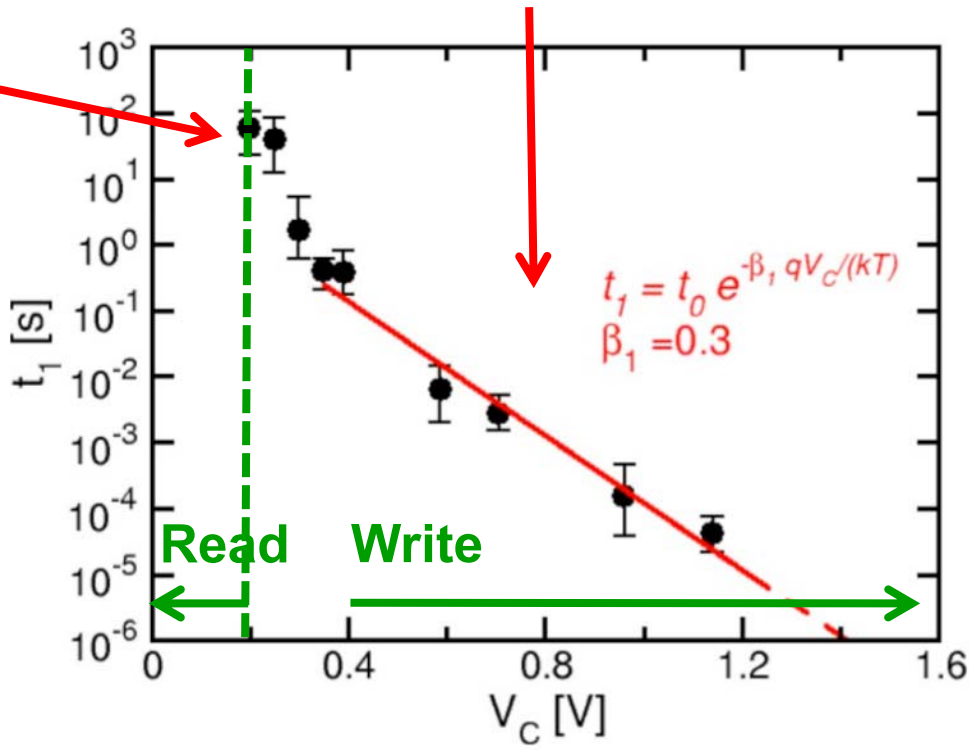
Adapted from R. Waser, MRS Spring Meeting 2009 RRAM Tutorial.

Building a filament: voltage, time & charge

- **Total charge transferred in time t is $Q_0 = jtA_{eff}$**
  - **A_{eff} is the effective area of the electrodeposit**
  - **$j = j_0 \exp(\alpha q V_c / kT)$**

$t_{prog} = Q_0 / [\, j_0 \exp(\alpha q V_c / kT)\, A_{eff}\,]$

Saturation at low voltage (nucleation overpotential, work function difference, , etc.?)



Q_0 is in the fC range (from electrodeposit volume) - gives programming energy in the order of fJ…

j_0=exchange current density, α =transfer coefficient, q=cation charge, V_c= cell voltage

U. Russo, D. Kamalanathan, D. Ielmini, A.L. Lacaita, and M.N. Kozicki, "Study of Multilevel Programming in Programmable Metallization Cell (PMC) Memory," IEEE Transactions on Electron Devices, Vol. 56, 1040 – 1047 (2009).

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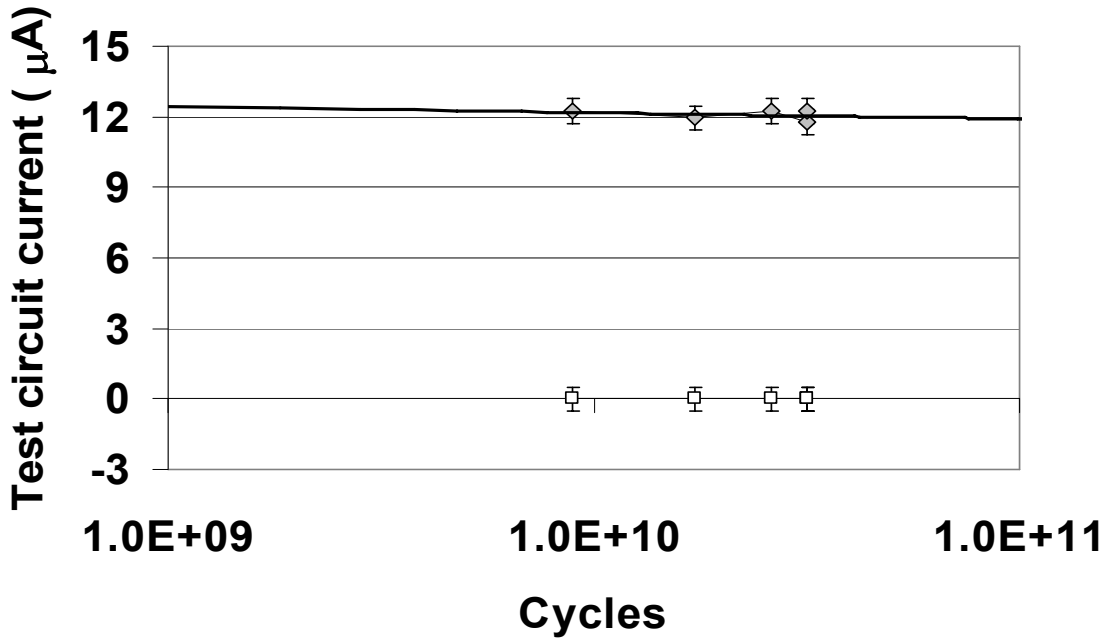
Endurance and retention

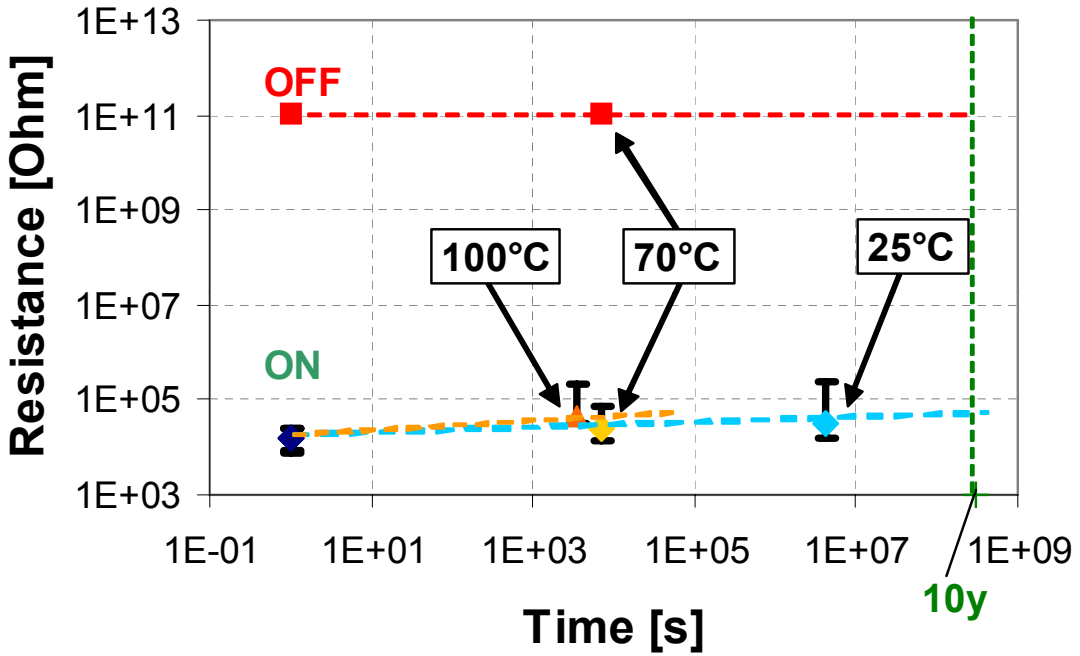
Endurance >10^{10} cycles with no degradation evident for 75 nm Ag-Ge-Se device (I_{prog}= 12 µA)

M.N. Kozicki, M. Park, and M. Mitkova, "Nanoscale Memory Elements Based on Solid-State Electrolytes," IEEE Trans. Nanotechnology, vol. 4, 331-338 (2005).

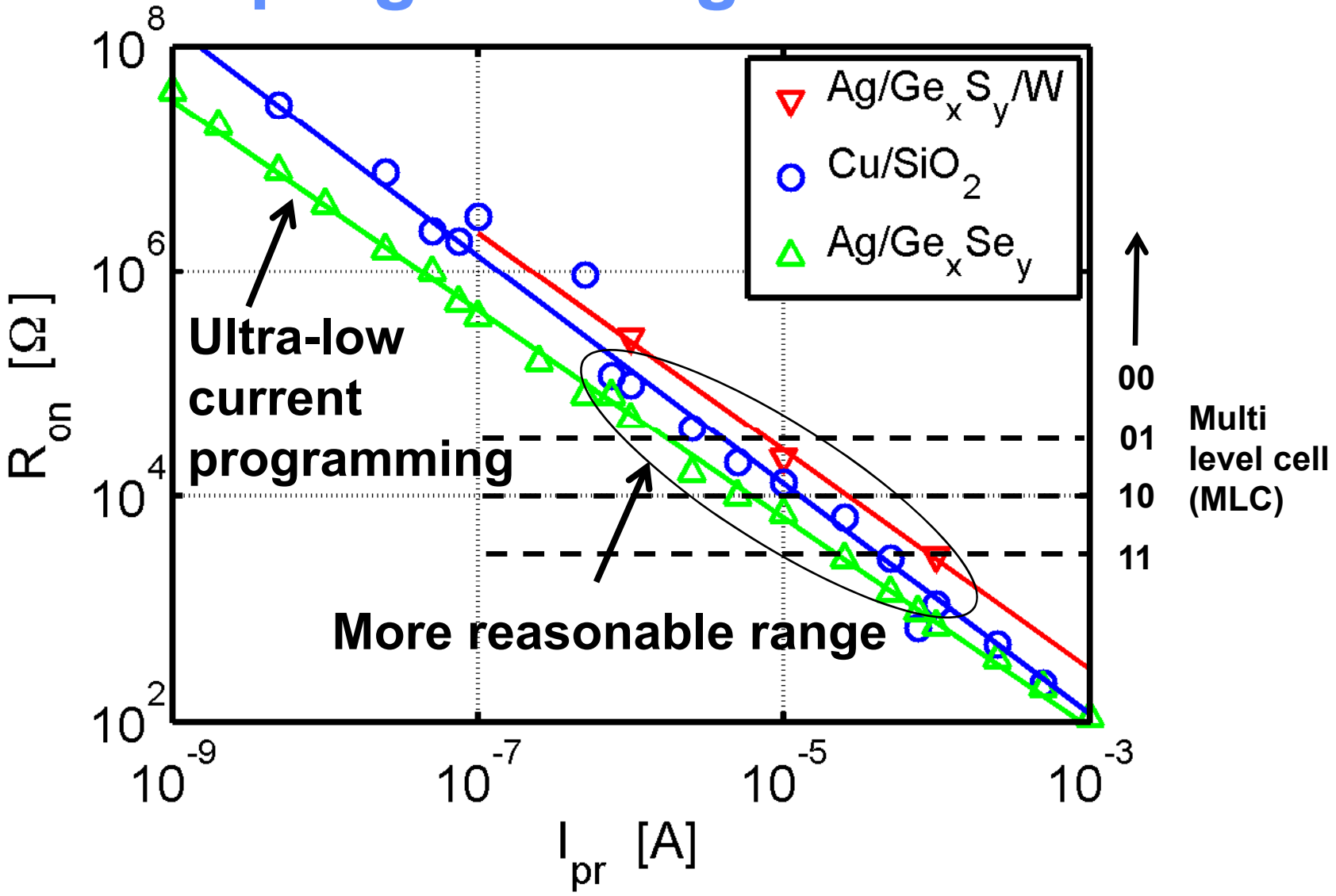


Retention >10 yrs at 100ºC for 90 nm Ag-Ge-S device (full wafer results)

R. Symanczyk, „Conductive Bridging Memory Development from Single Cells to 2Mbit Memory Arrays", 8th Non-Volatile Memory Technology Symposium, 2007.

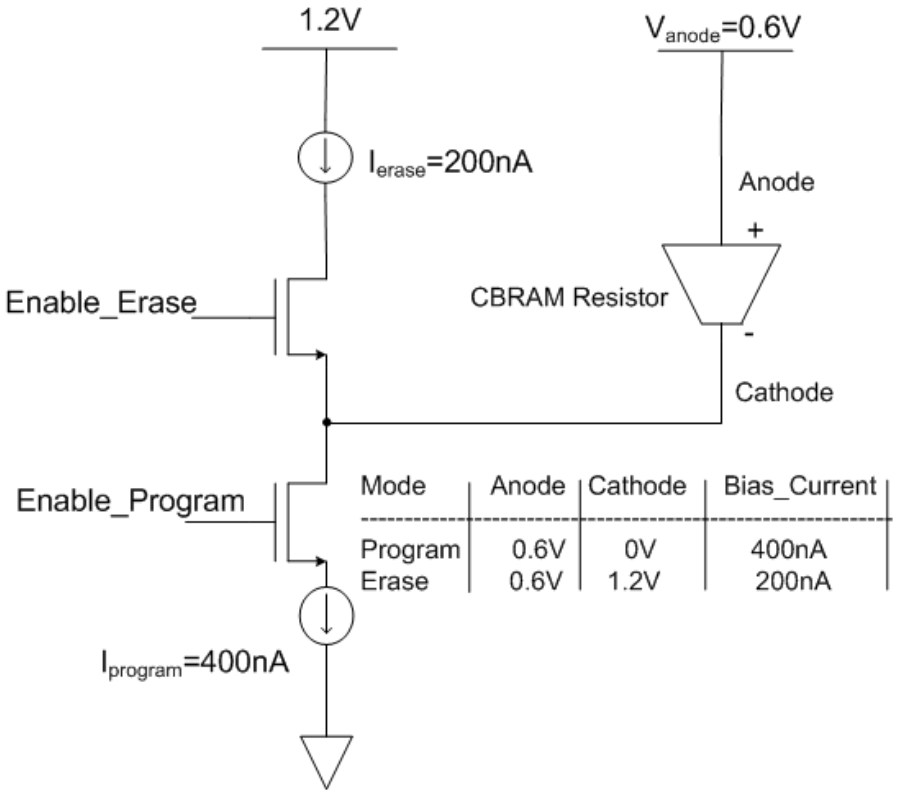


On-state resistance vs. programming current

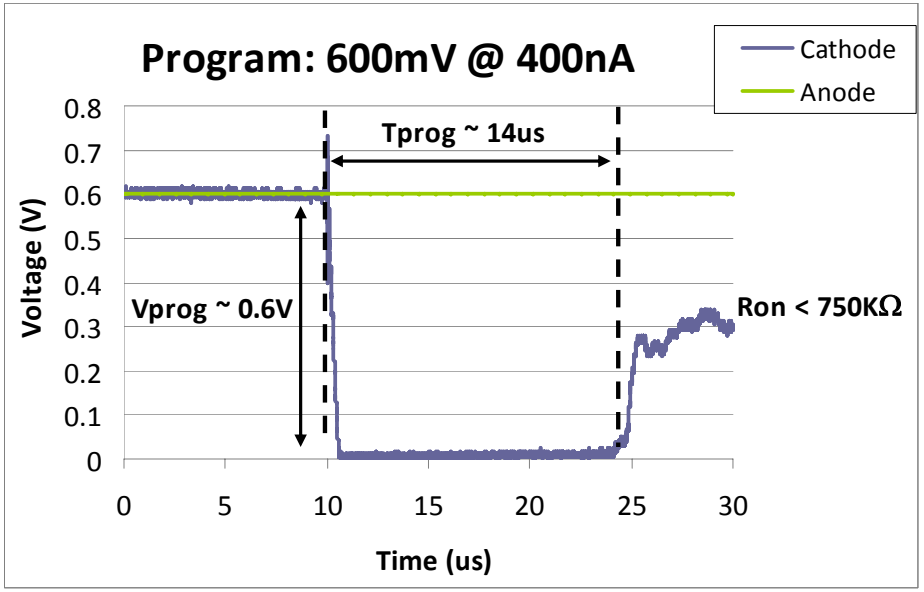


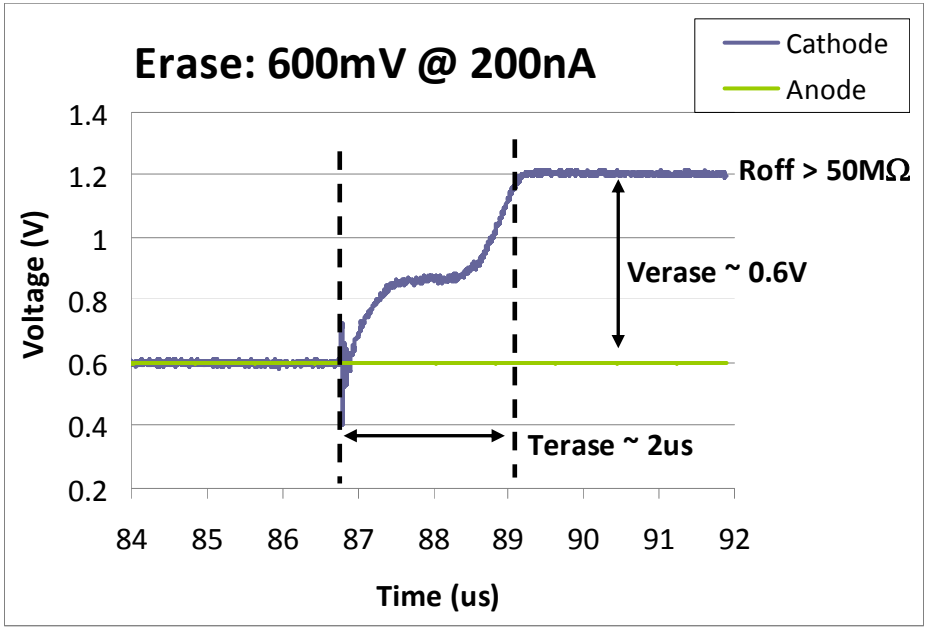
Data compiled by John Jameson, Adesto Technologies. Some data taken from R. Waser, R. Dittmann, G. Staikov, and K. Szot, "Redox-Based Resistive Switching Memories – Nanoionic Mechanisms, Prospects, and Challenges", Adv. Mater., Vol. 21, 2632–2663 (2009).

Low voltage operation



Mode	Anode	Cathode	Bias_Current
Program	0.6V	0V	400nA
Erase	0.6V	1.2V	200nA

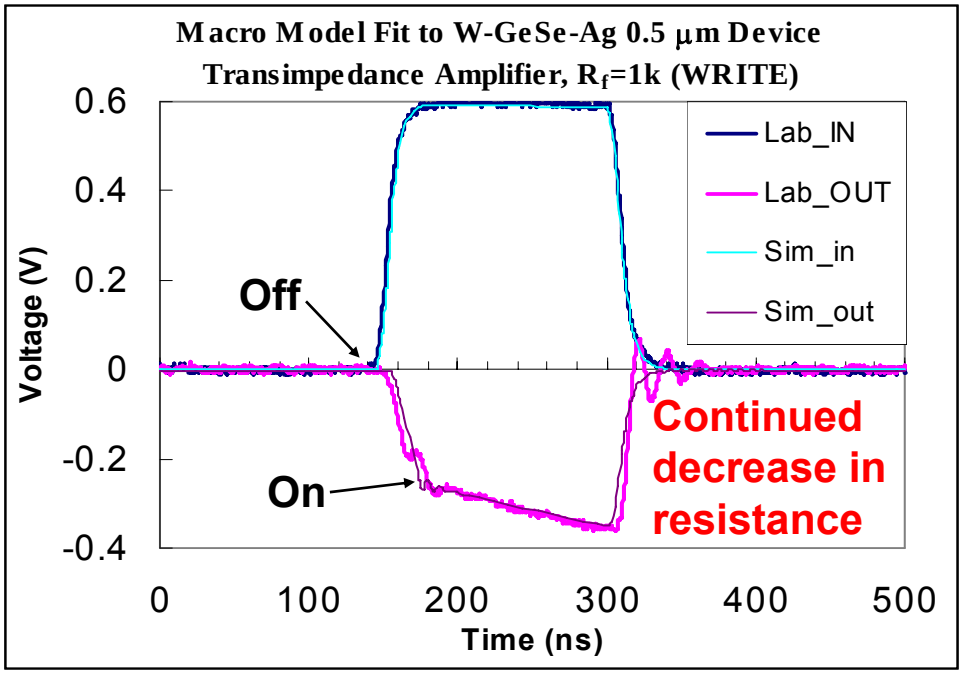


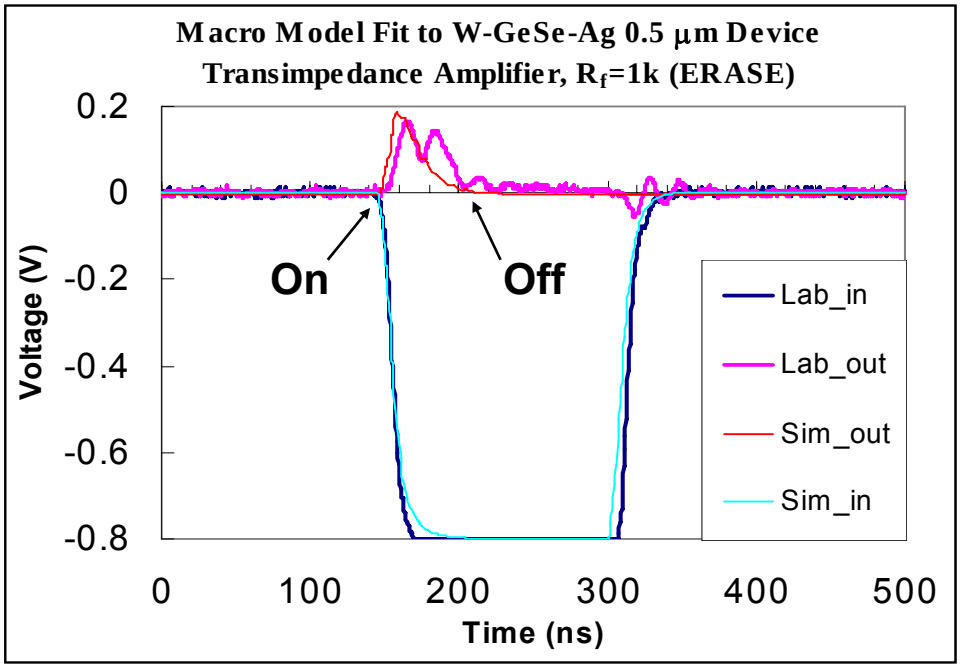


600 mV, 400/200 nA operation
3.36 pJ write, 240 fJ erase

N. Derhacobian, S.C.Hollmer, N. Gilbert, M.N. Kozicki, “Power and Energy Perspectives of Nonvolatile Memory Technologies,” Proc. IEEE, vol. 98, 283-298 (2010).

Dynamic (pulse) programming of Ag-Ge-Se devices



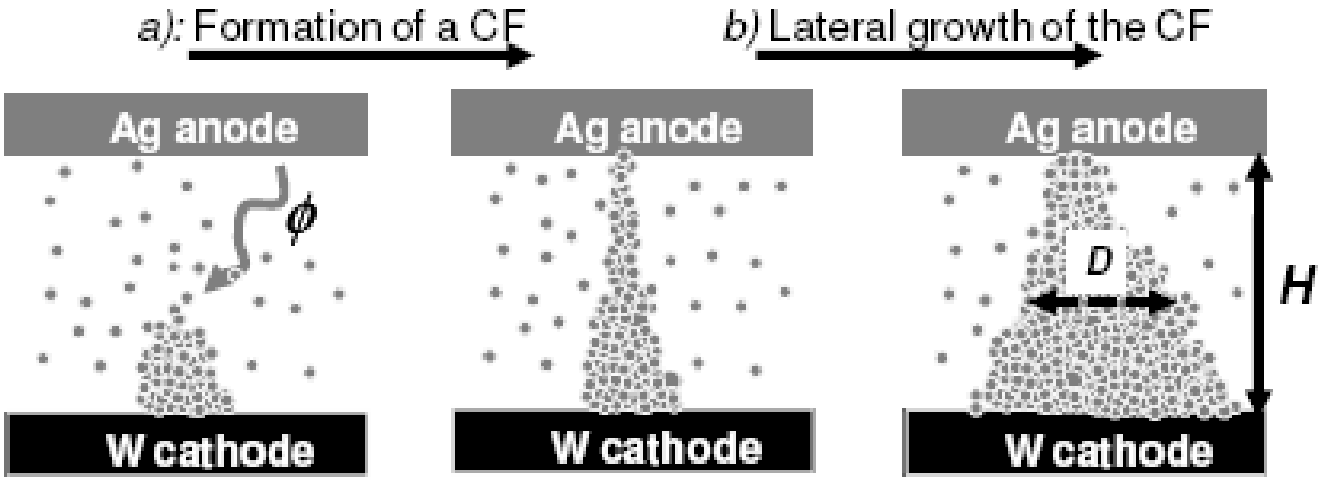


Write **Erase**

Output signal is via a transimpedance amplifier so that increasing voltage magnitude means increasing current (or decreasing device resistance)

N. Gilbert, C. Gopalan, and M. N. Kozicki, "A Macro model of Programmable Metallization Cell Devices," Solid State Electronics, vol. 49, 1813-1819 (2005).

Schematic diagram of two-stage conducting filament formation process

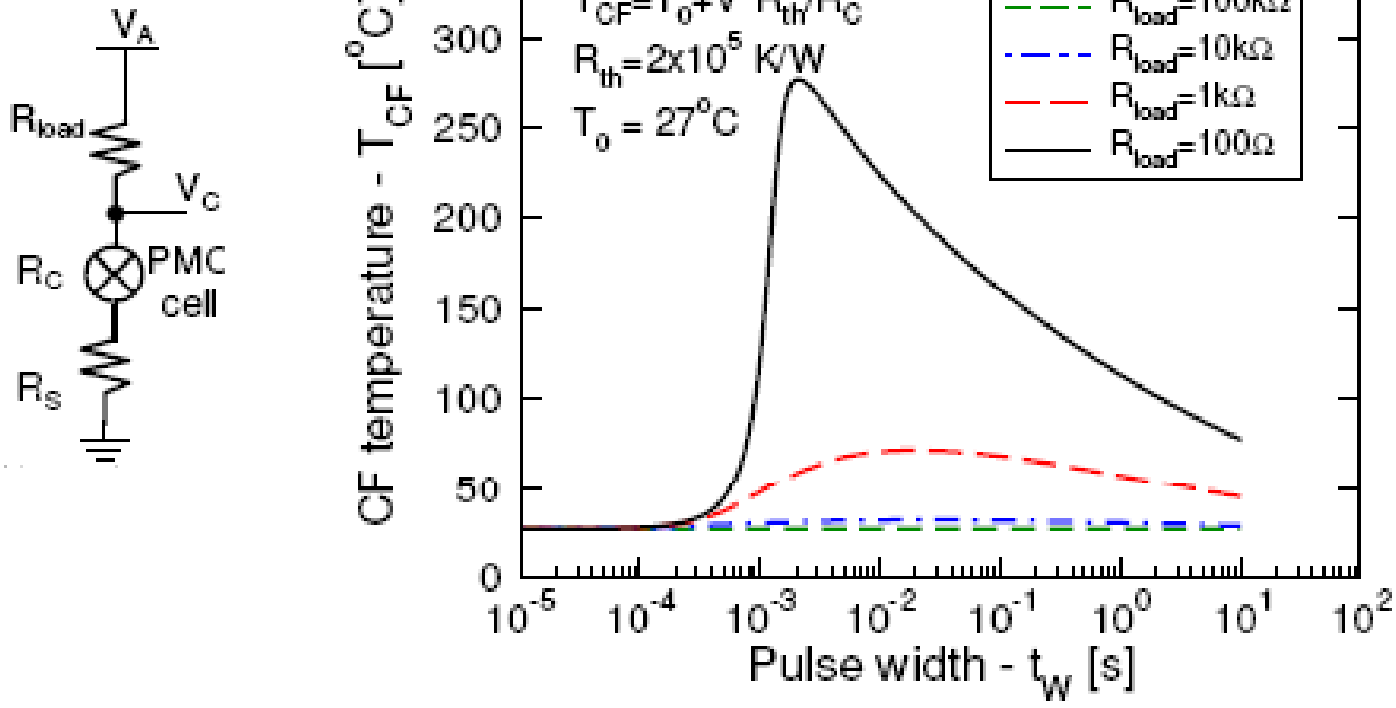


Both the *initial formation* and *radial growth* are driven by ion migration

But… is this everything?

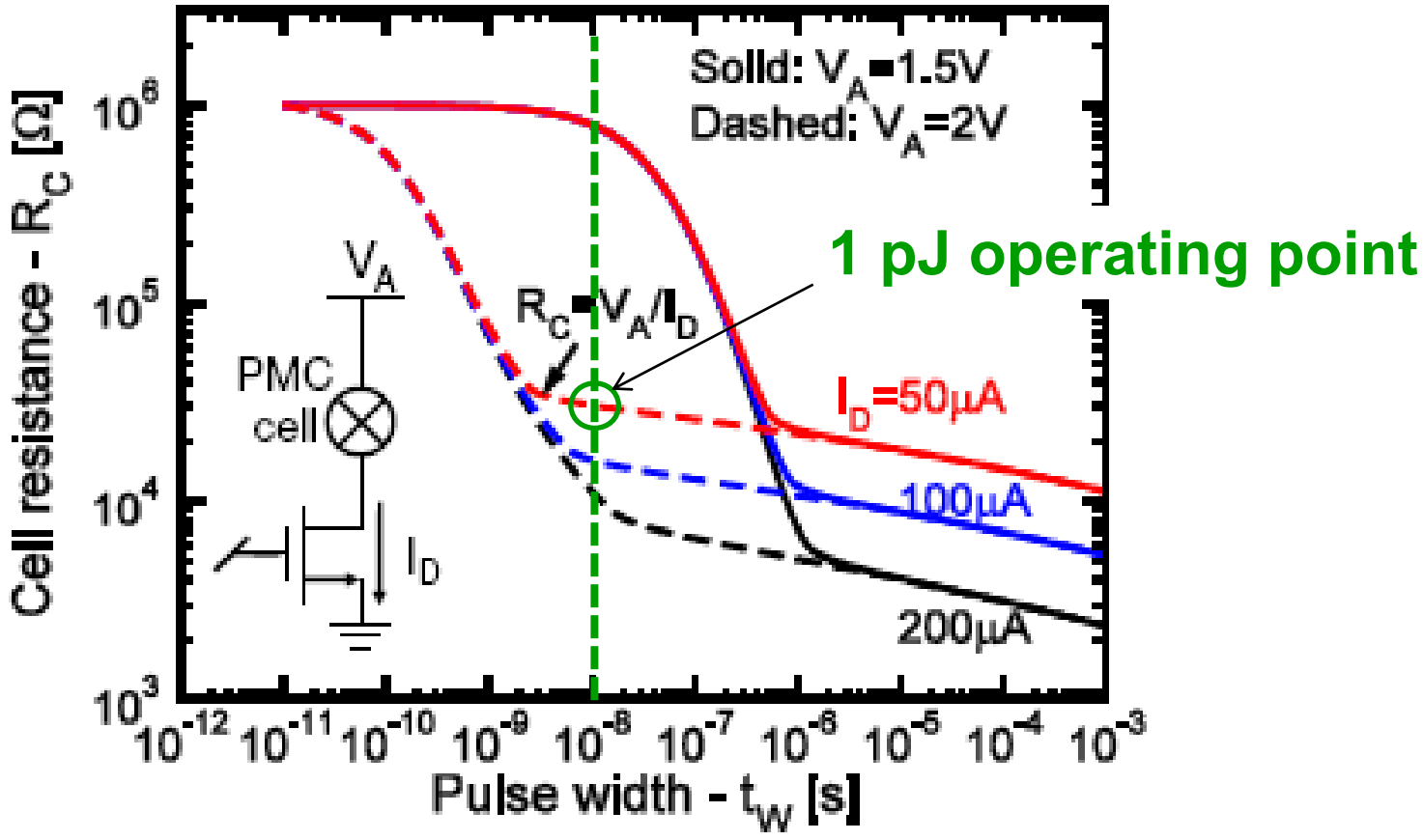
U. Russo, D. Kamalanathan, D. Ielmini, A.L. Lacaita, and M.N. Kozicki, "Study of Multilevel Programming in Programmable Metallization Cell (PMC) Memory," IEEE Transactions on Electron Devices, Vol. 56, 1040 – 1047 (2009).

Joule heating during programming with high currents



- **Joule heating is evident at low R_{load}/high current**
- **Maximum temperature rise for 1 kΩ load is 40ºC**

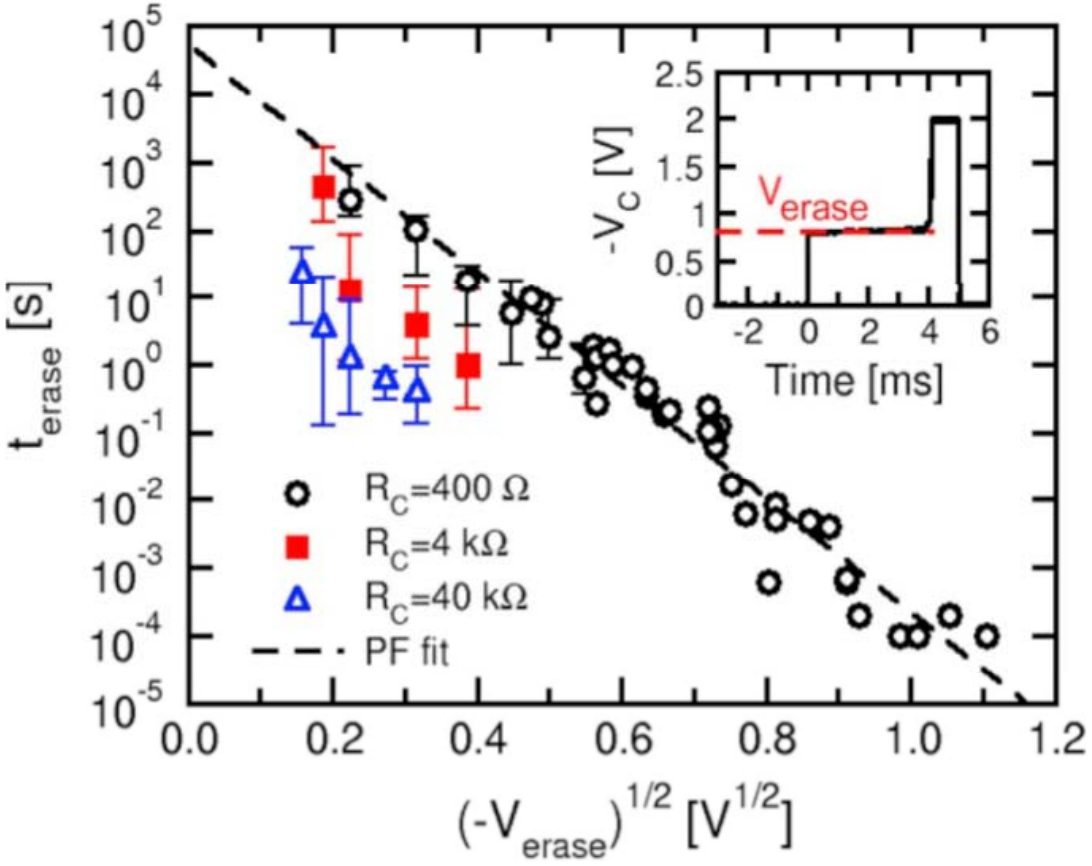
Conservative programming model



Model is based on a Ag/Ag-Ge-S/W 1T-1R cell and includes transistor load and Joule heating effects

U. Russo, D. Kamalanathan, D. Ielmini, A.L. Lacaita, and M.N. Kozicki, "Study of Multilevel Programming in Programmable Metallization Cell (PMC) Memory," IEEE Transactions on Electron Devices, Vol. 56, 1040 – 1047 (2009).

Erase kinetics



Erase time defined by 10x increase in resistance

D. Kamalanathan, U. Russo, D. Ielmini, and M.N. Kozicki, "Voltage-Driven On–Off Transition and Tradeoff With Program and Erase Current in Programmable Metallization Cell (PMC) Memory," IEEE Electron Device Letters, Vol. 30, 553 – 555 (2009).

- No exponential is forever…
- The need for new memory
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- Introduction to ionic memory
- Device characteristics and models
- **Materials at the nanoscale**
- Active and passive arrays
- Real stuff
- Questions and discussion

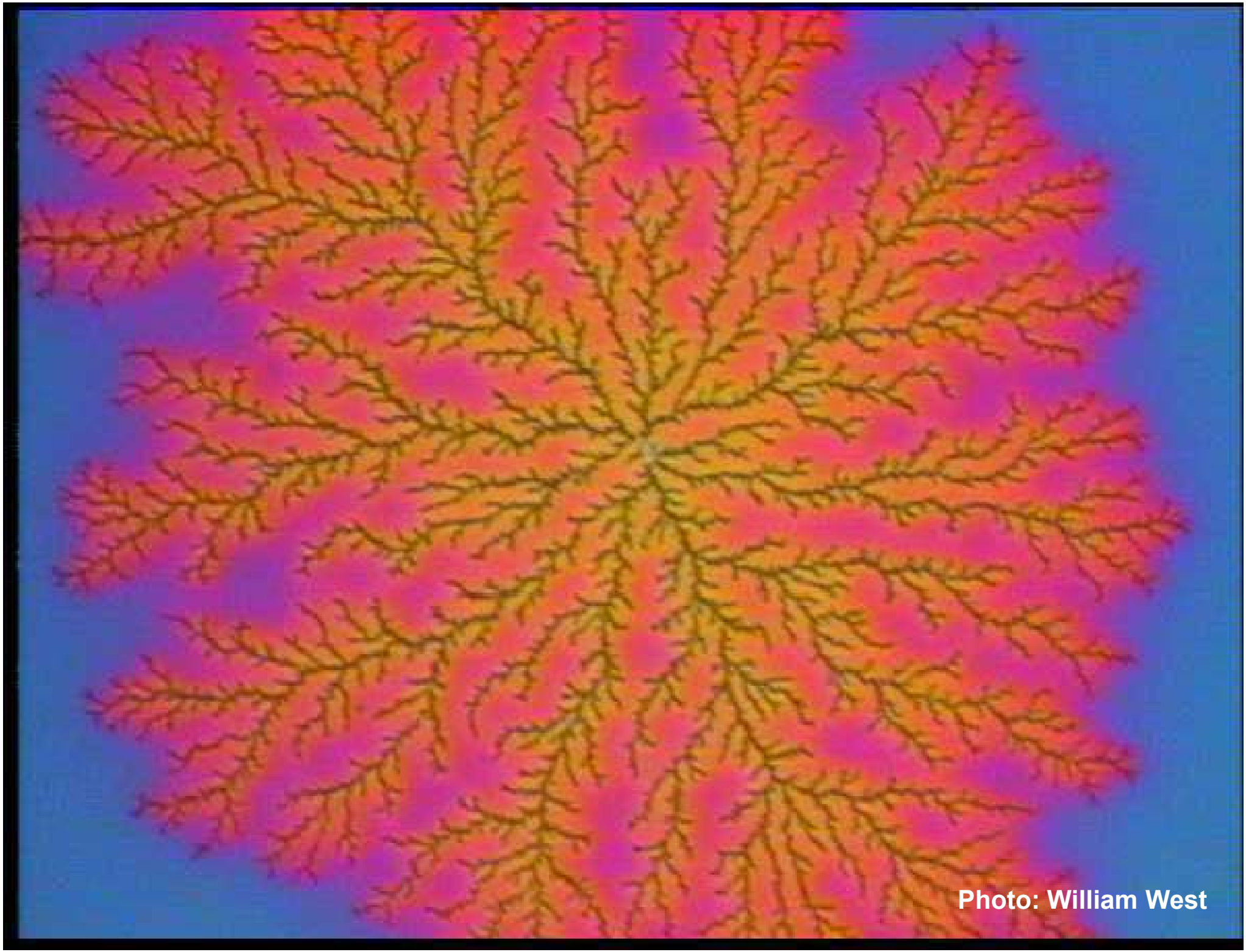
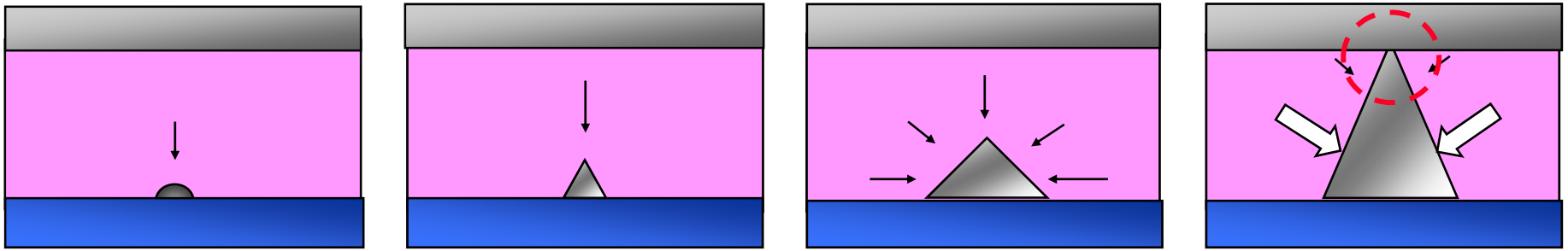


Photo: William West


Photo: Chakku Gopalan

Electrodeposit evolution in a homogeneous solid electrolyte



1,2D nucleation | Outward growth | 3D growth | Constrained 3D growth

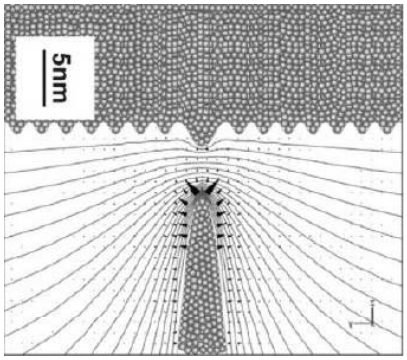
Growth speed of a (cylindrical) nanofilament

$$\dot{h}[\mathrm{cm/s}] = \frac{M_A}{\pi r^2 z N_A e_0 \rho} I[\mathrm{A}]$$

M_A=atomic mass
N_A=Avogadro's #
Ze_0=charge on ion
ρ=filament density
r=filament radius

Example: Ag filament of 10nm diameter at *I* = 1 μA

$$\rightarrow \dot{h} \sim 1.3\,\mathrm{m/s}$$



Erase initiation via potential concentration at tip of electrodeposit

X. Guo, C. Schindler, S. Menzel, and R. Waser, "Understanding the switching-off mechanism in Ag^+ migration based resistively switching model systems," Appl. Phys. Lett., Vol. 91, 133513 (2007).

Adpted from R. Waser, MRS Spring Meeting 2009 RRAM Tutorial.

Where do the metallic filaments form?

Jaakko Akola
University of Jyväskylä and Tampere Technological University, Finland

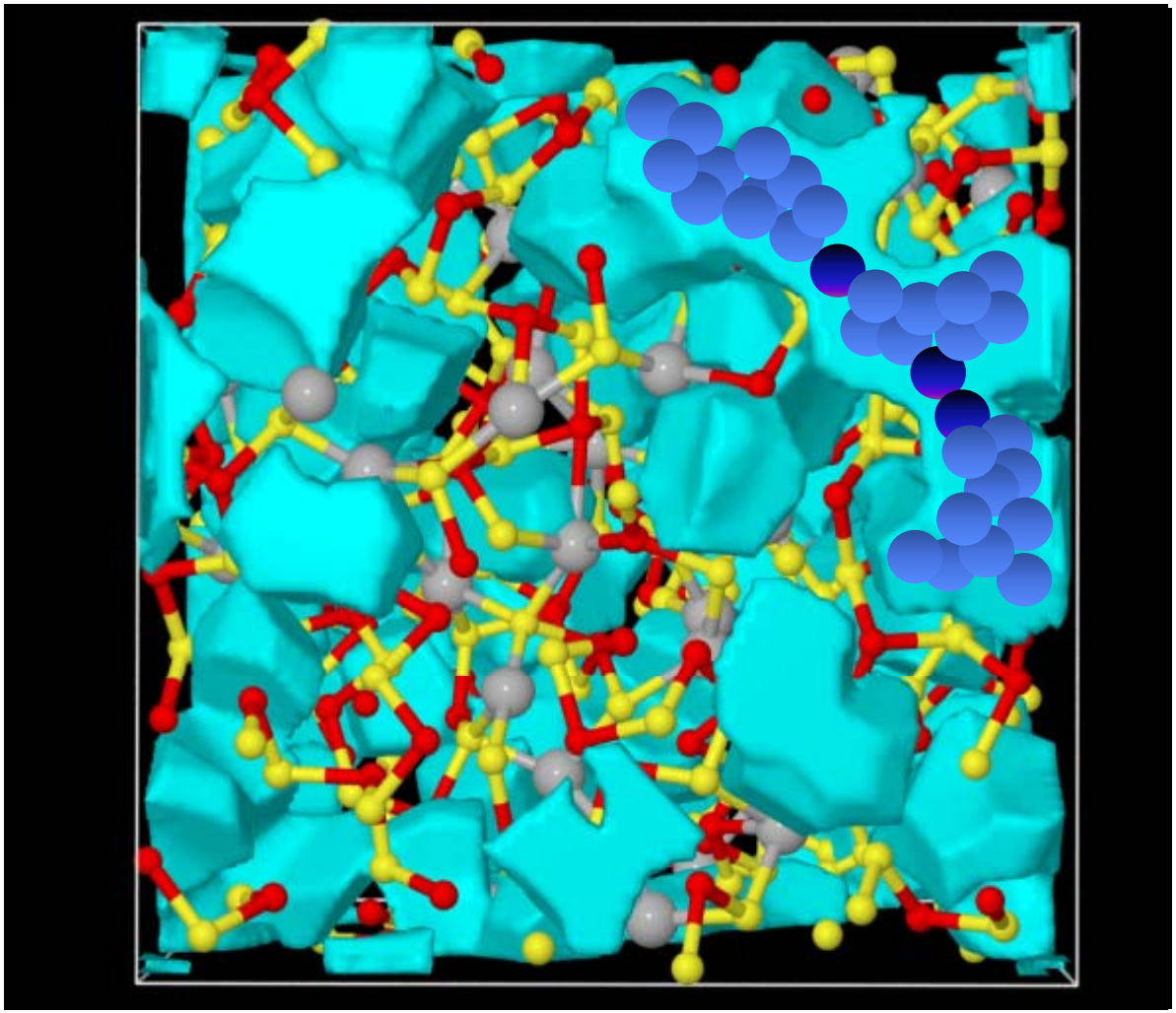
Bob Jones
Jülich Research Center, Germay

Tomas Wagner
University of Pardubice, Czech Republic

Techniques:

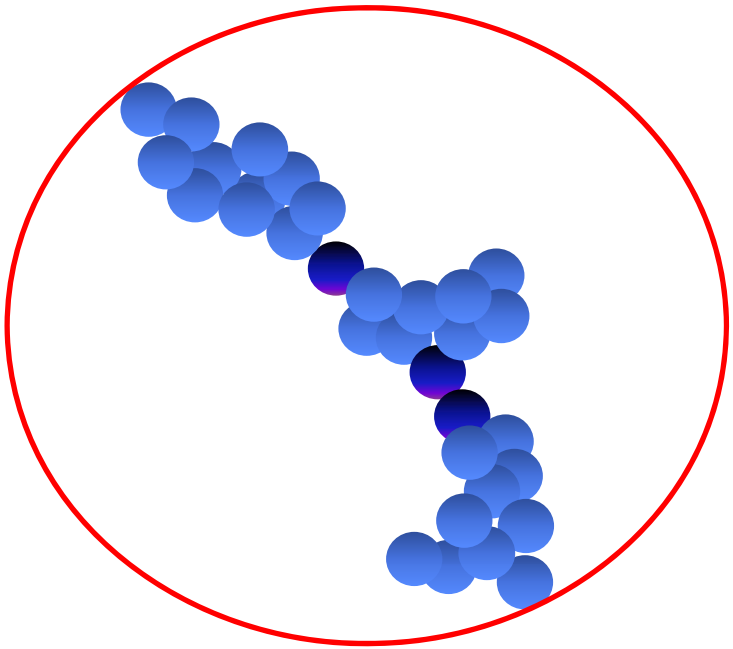
Full DFT, 500 atom system

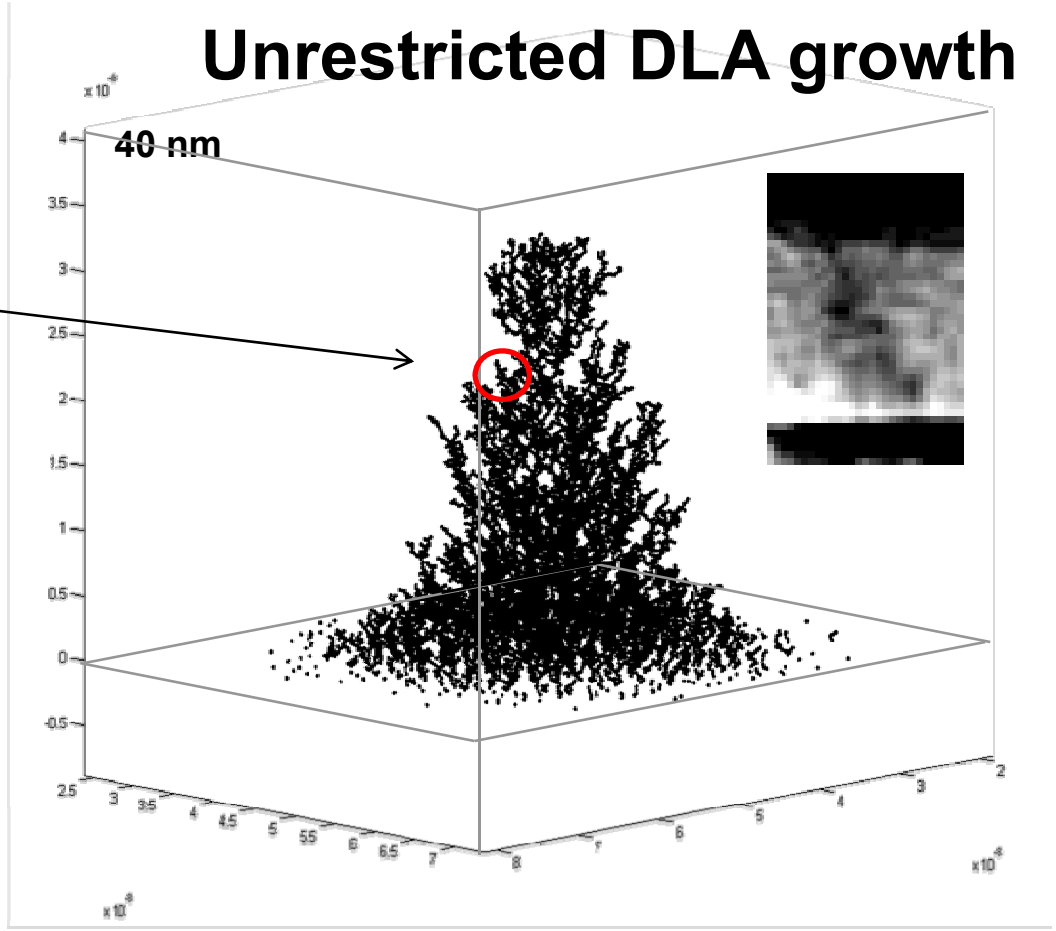
X-ray diffraction, neutron scattering, EXAFS



Cavities comprise 24% of the volume of $Ag_{12}As_{35}S_{53}$, (SiO_2 is 32% but cavities are more dispersed?)

Filament morphology





Full filament may be composed of few to many nano-filaments in parallel.

Rainer Waser
RWTH Aachen and Jülich Research Center, Germany

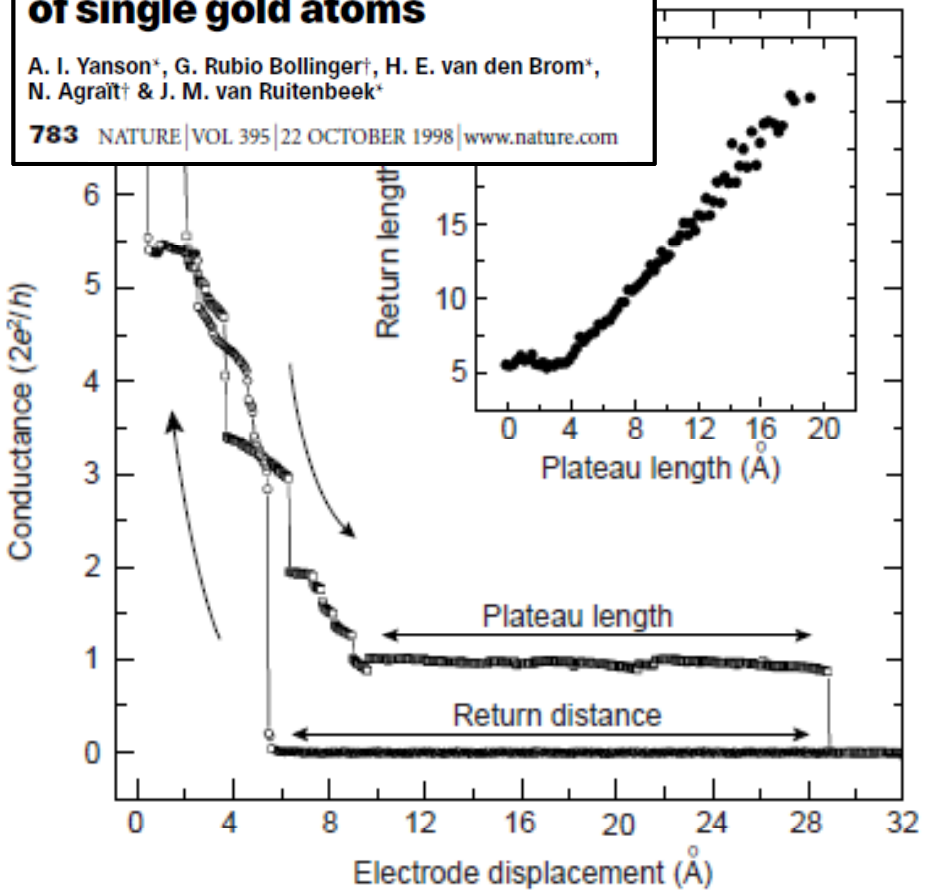
Resistance in atomic-scale wires

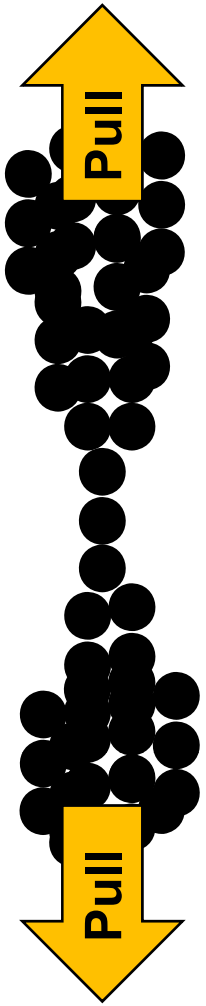
Conductance quantized in units of $2e^2/h$ (R = 12.9kΩ)

Formation and manipulation of a metallic wire of single gold atoms

A. I. Yanson*, G. Rubio Bollinger†, H. E. van den Brom*, N. Agraït† & J. M. van Ruitenbeek*

783 NATURE | VOL 395 | 22 OCTOBER 1998 | www.nature.com

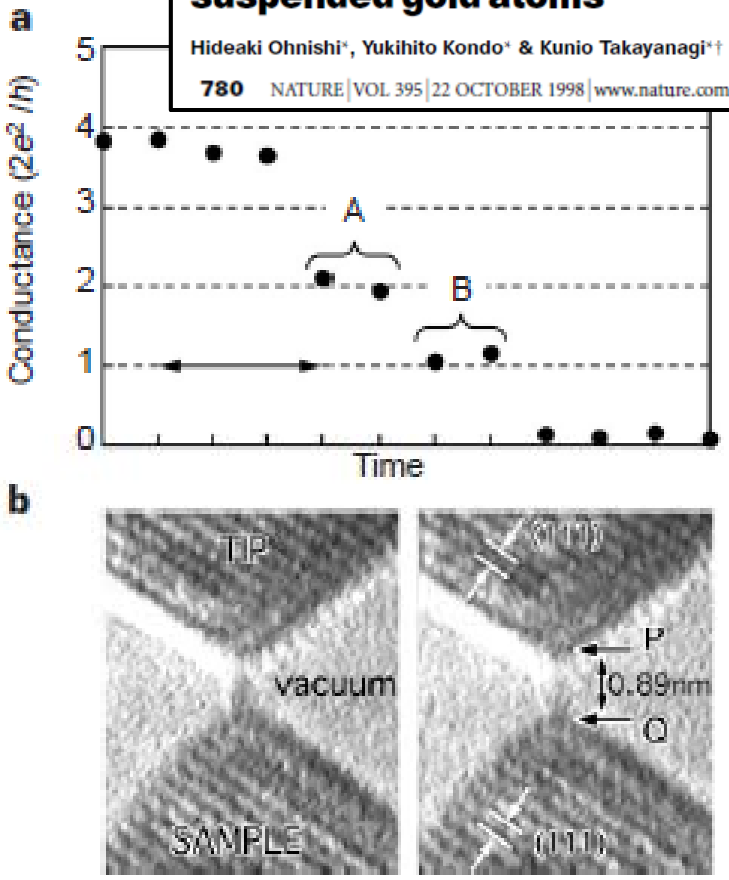




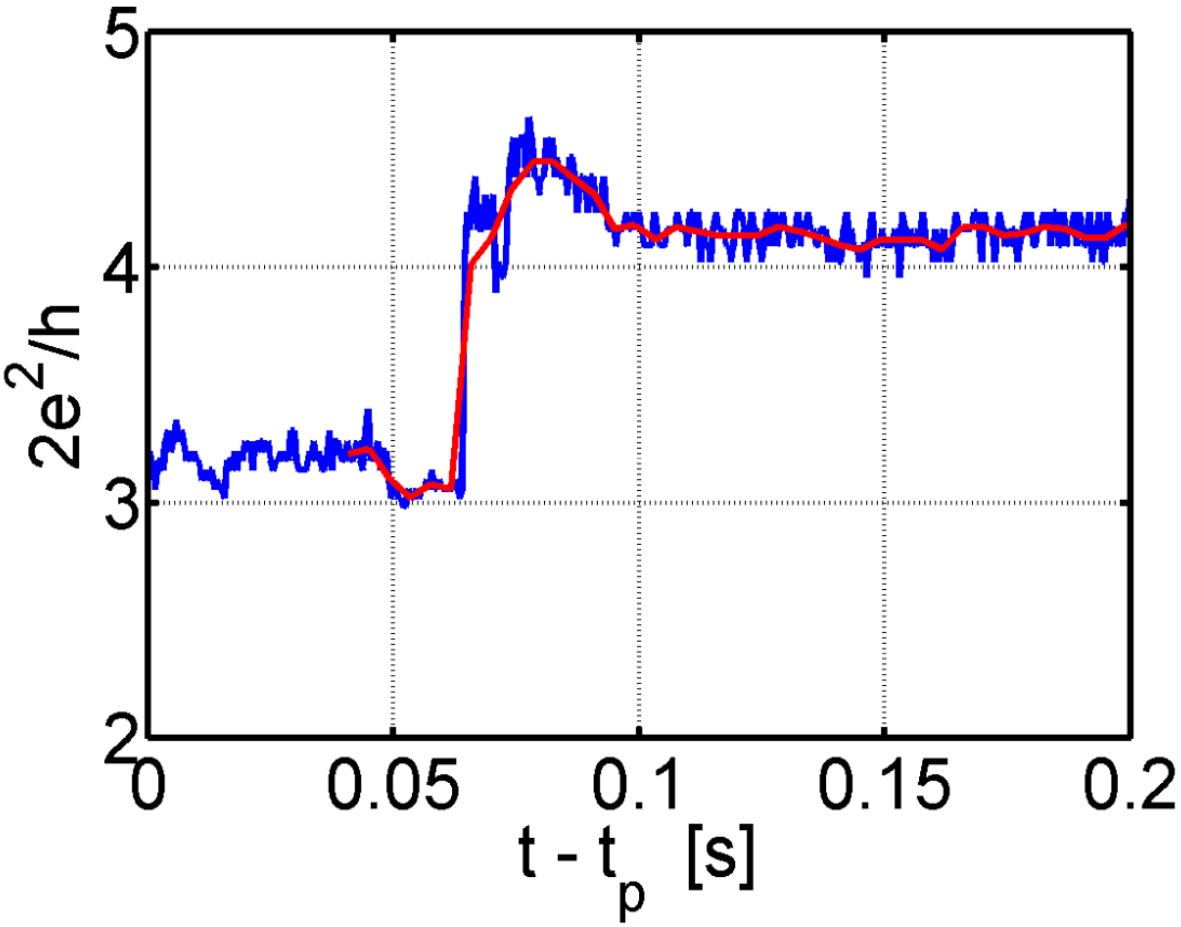
Quantized conductance through individual rows of suspended gold atoms

Hideaki Ohnishi*, Yukihito Kondo* & Kunio Takayanagi*†

780 NATURE | VOL 395 | 22 OCTOBER 1998 | www.nature.com



Quantized conductance in CBRAM



John Jameson, Adesto Technologies

Quantized conductance atomic switch

K. Terabe,*et al*., NIMS, Nature, vol. 433, p. 47 (2005).

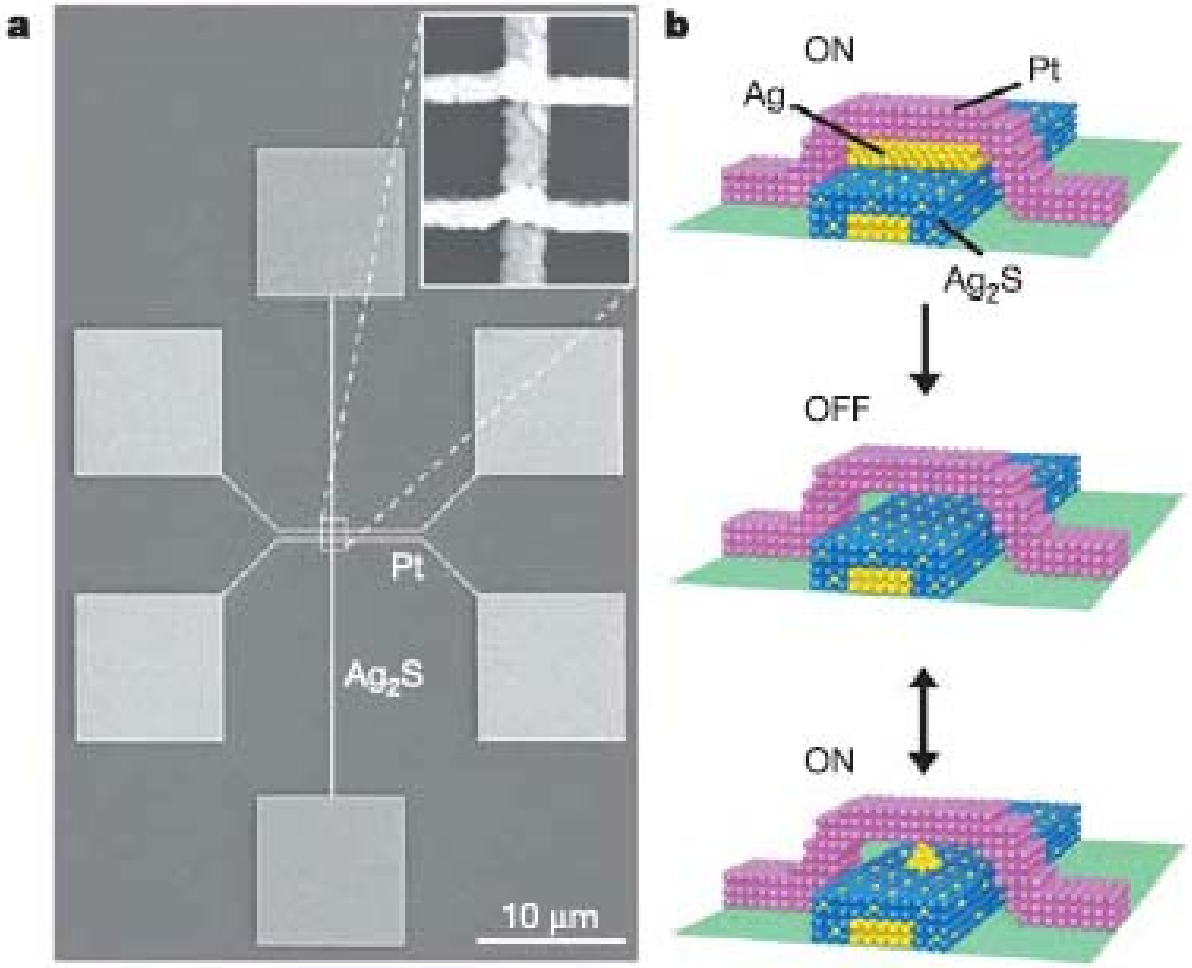


Figure 1 Basics of the QCAS. **a**, SEM image of the QCAS. A QCAS is formed at each crossing point of the 150-nm-wide Ag_2S wire and the two Pt wires of 100 nm width. **b**, Schematic diagrams of the QCAS. As-formed switched-on state (top), switched-off state (middle) and switched-on state after the initial switching-off process (bottom).

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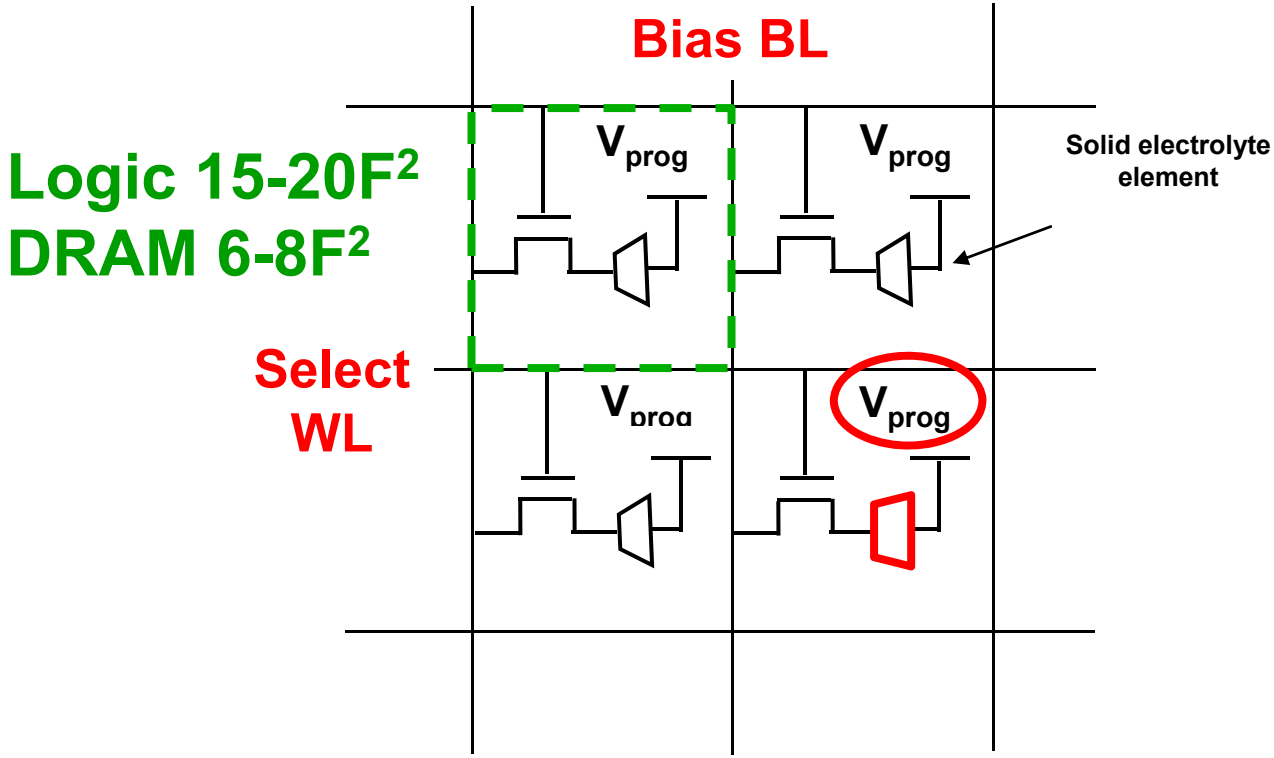
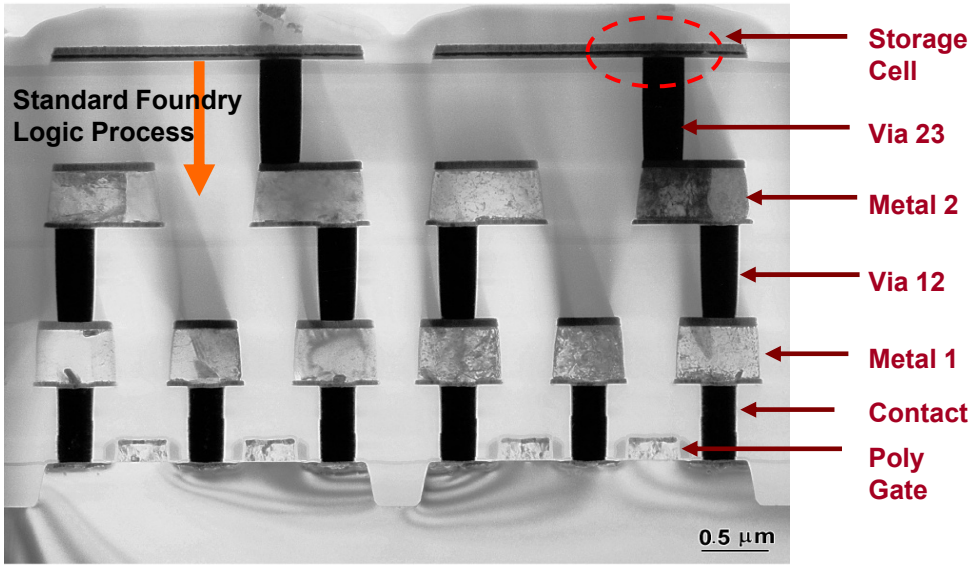
Array options

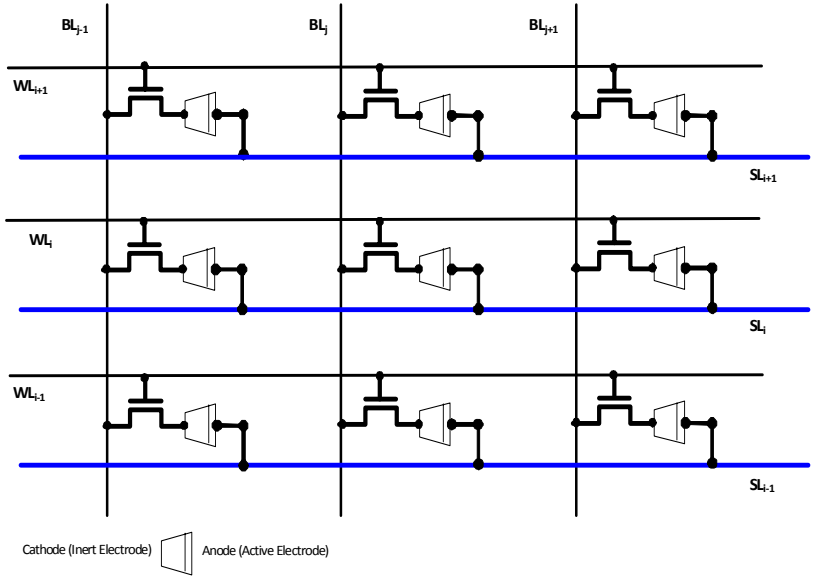
Active (1T-1R)

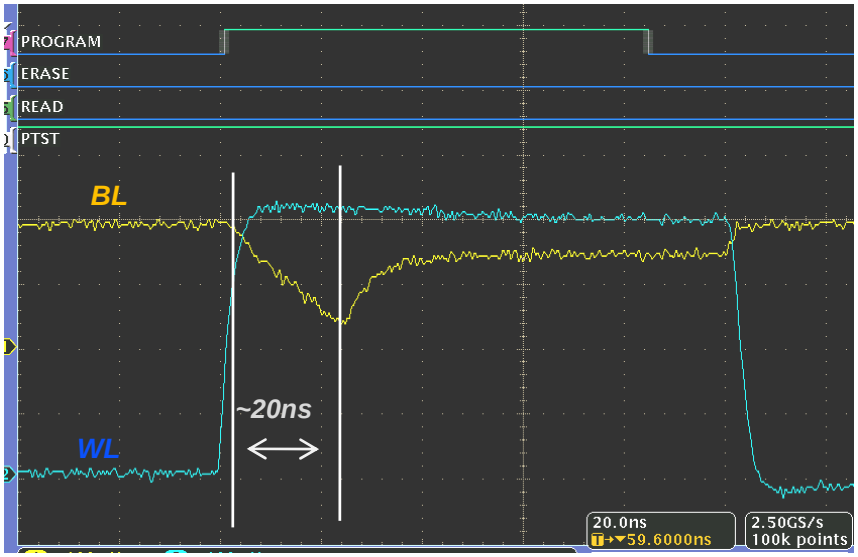


V_{prog} is above or below transistor drain voltage to program or erase selected cell, programming current via bit line (BL)

1T-1R array fabrication and performance

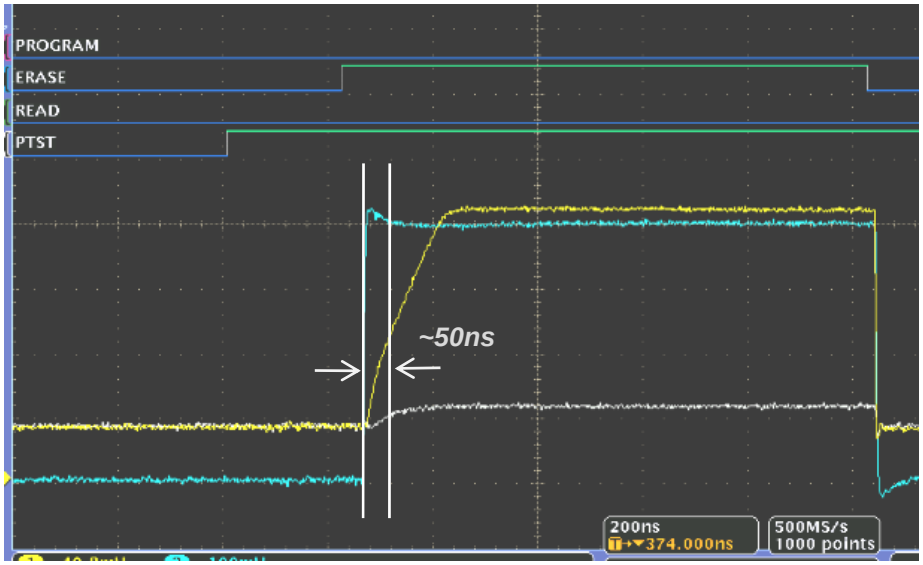






Program Operation (SET)

20 ns



Erase Operation (RESET)

50 ns

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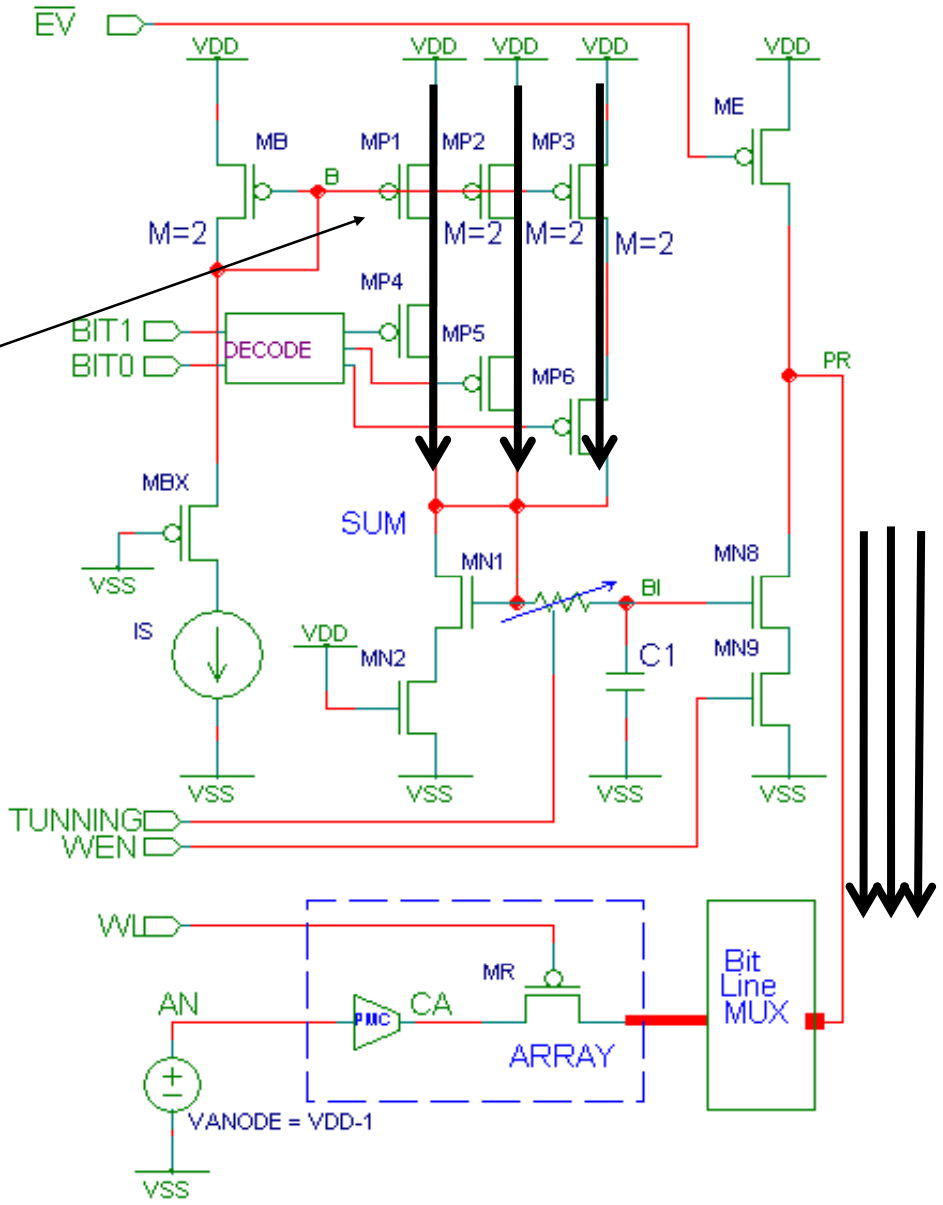
Multi-level cell (MLC) write

Three transistors are used to create three discrete current levels to set ON resistance (gives 4 resistance states = 2 bits).



N.E. Gilbert and M.N. Kozicki, *"An Embeddable Multilevel-Cell Solid Electrolyte Memory Array,"* IEEE Journal of Solid-state Circuits, vol. 42, no. 6, pp 1383-1391, June 2007

MLC read

Current comparators used to sense device current

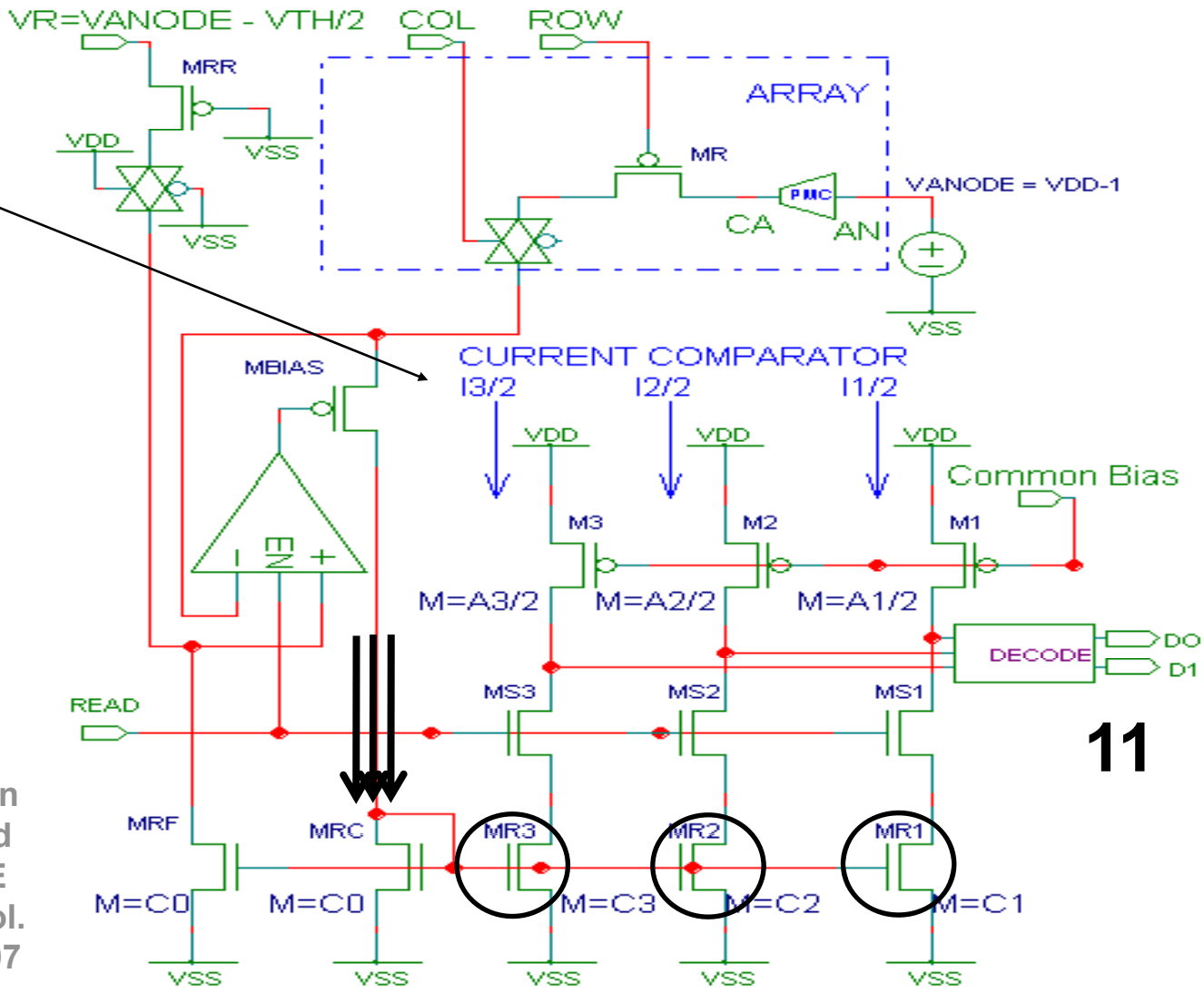
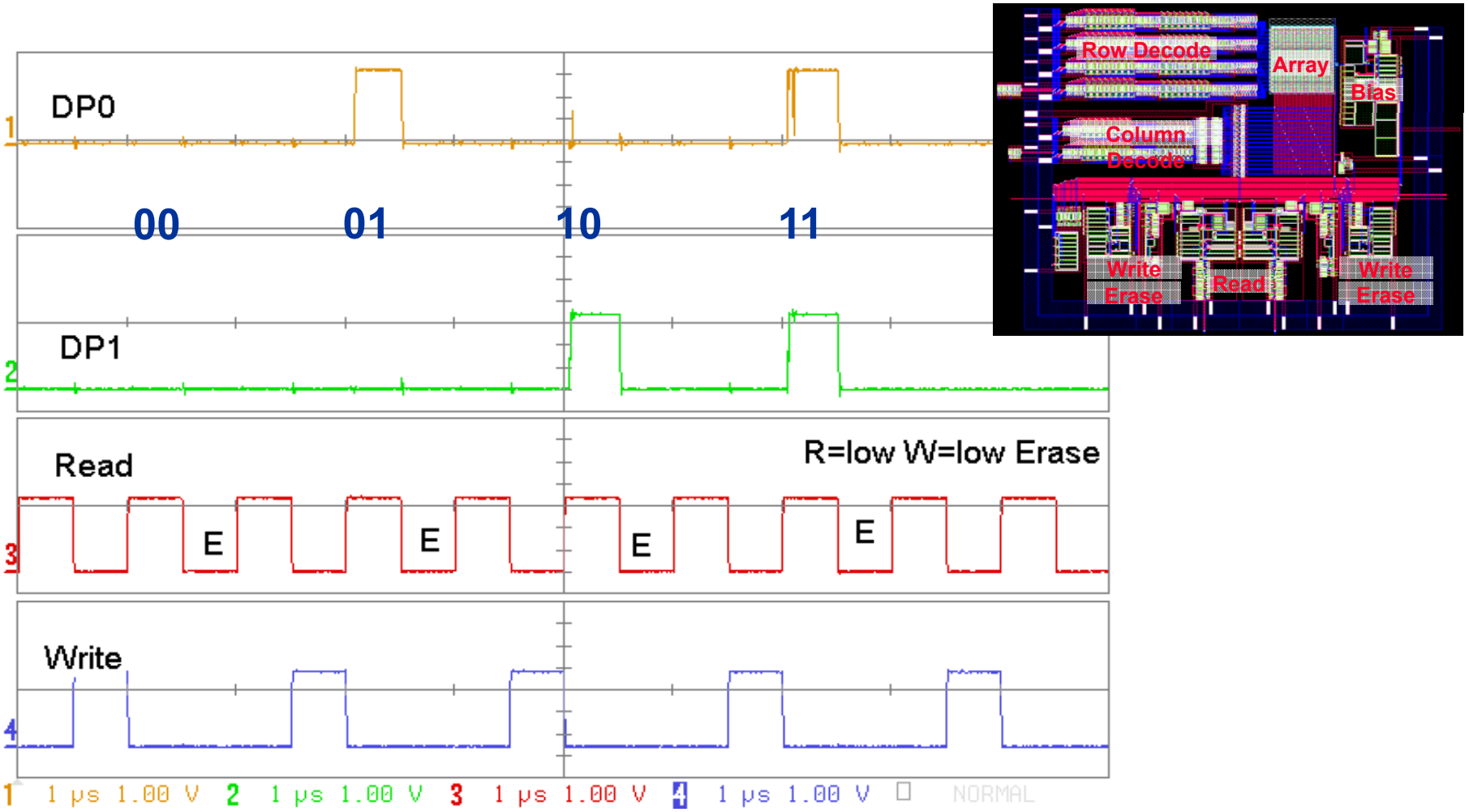


Fig. 3. Read circuit for multi-bit per cell implementations.

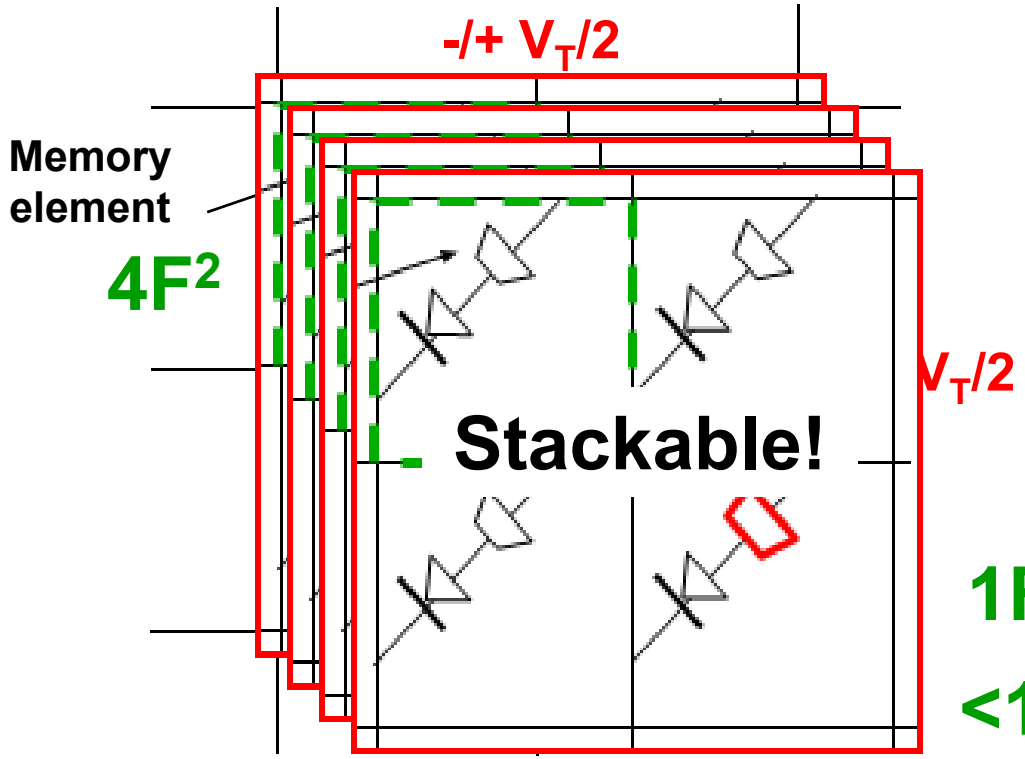
N.E. Gilbert and M.N. Kozicki, *"An Embeddable Multilevel-Cell Solid Electrolyte Memory Array,"* IEEE Journal of Solid-state Circuits, vol. 42, no. 6, pp 1383-1391, June 2007

MLC array operation



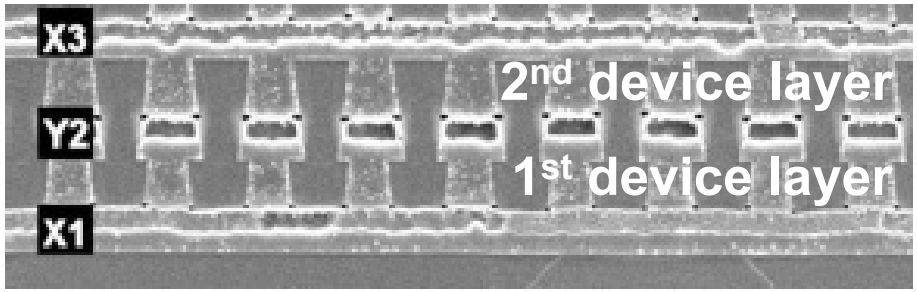
N.E. Gilbert and M.N. Kozicki, *"An Embeddable Multilevel-Cell Solid Electrolyte Memory Array,"* IEEE Journal of Solid-state Circuits, vol. 42, no. 6, pp 1383-1391, June 2007

Benefits of passive arrays

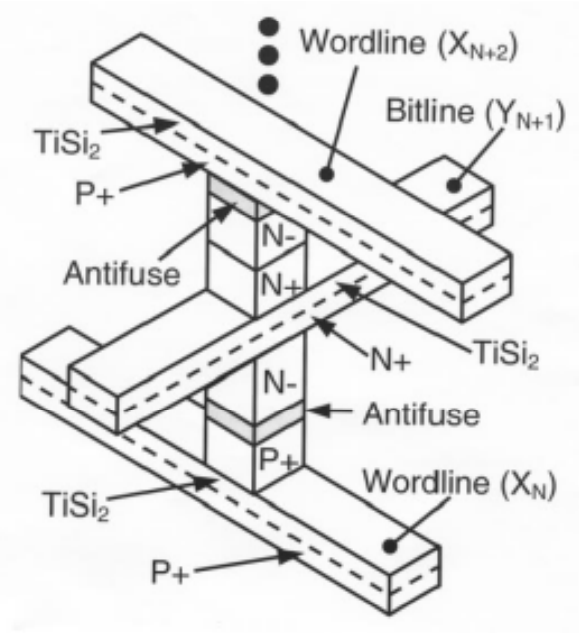


Selected cell has +/-half threshold voltage on row and -/+half on column for write or erase

Example of multi-layer approach



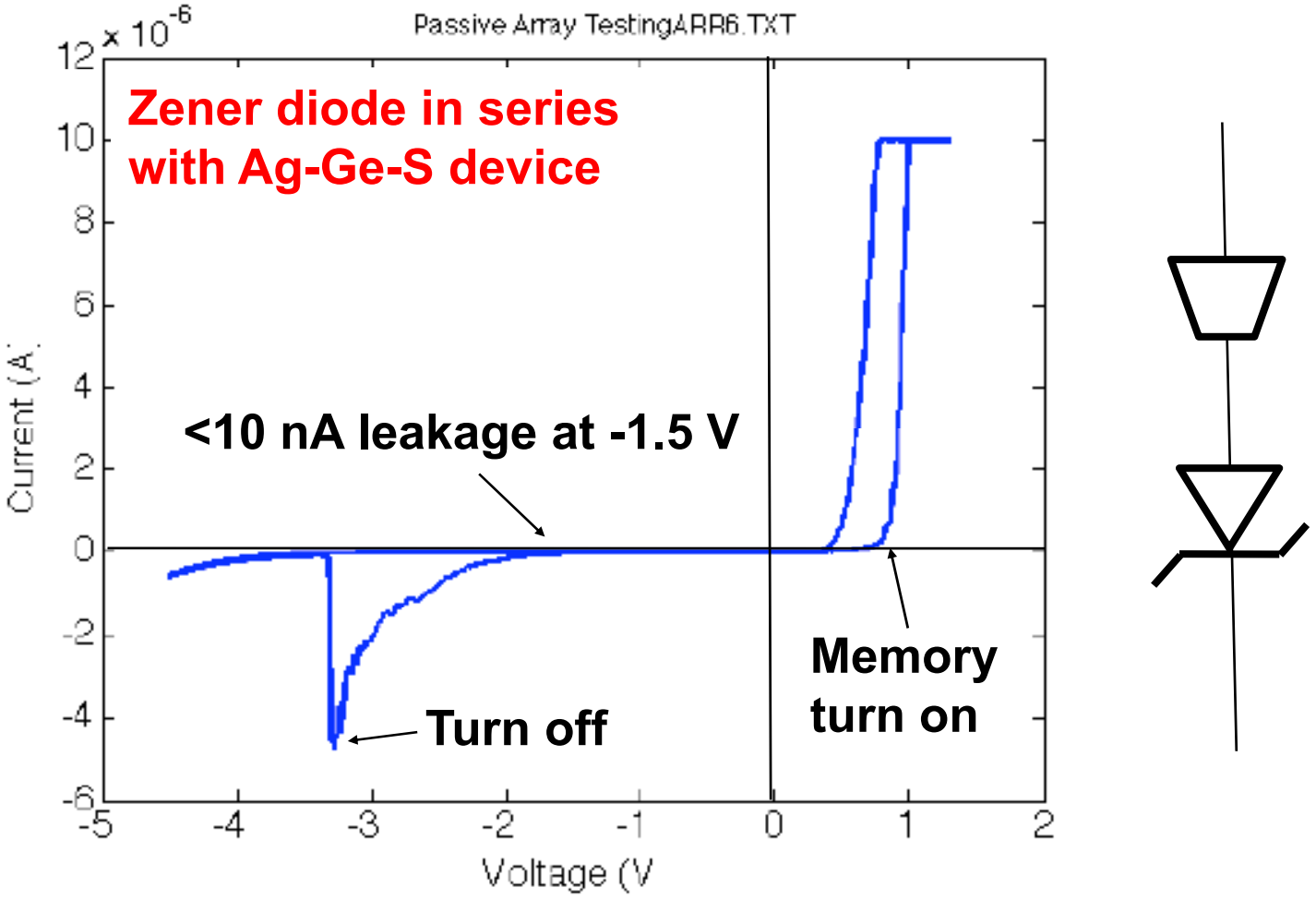
Example (from Matrix Semiconductor) showing diode isolation in a passive array of OTP structures



Solid electrolyte devices are compatible with such 3-D approaches, although passive arrays require *unipolar* programming or *Zener diode* isolation

M. Johnson *et al*., *"512-Mb PROM With a Three-Dimensional Array of Diode/Antifuse Memory Cells*," IEEE Journal of Solid-state Circuits, vol. 11, no. 38, 1920-1928, 2003

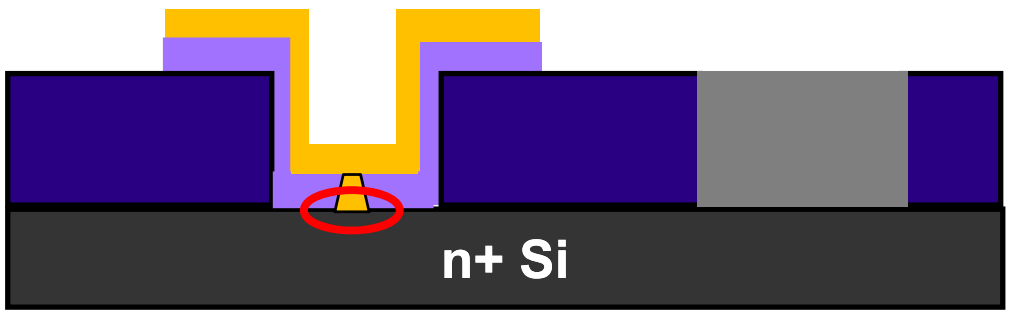
Discrete diode isolation



Data from Sarath C. Puthen Thermadam, ASU

See also H. Toda (Toshiba), US Patent #7,606,059, October 20, 2009

Integrated diode isolation - write

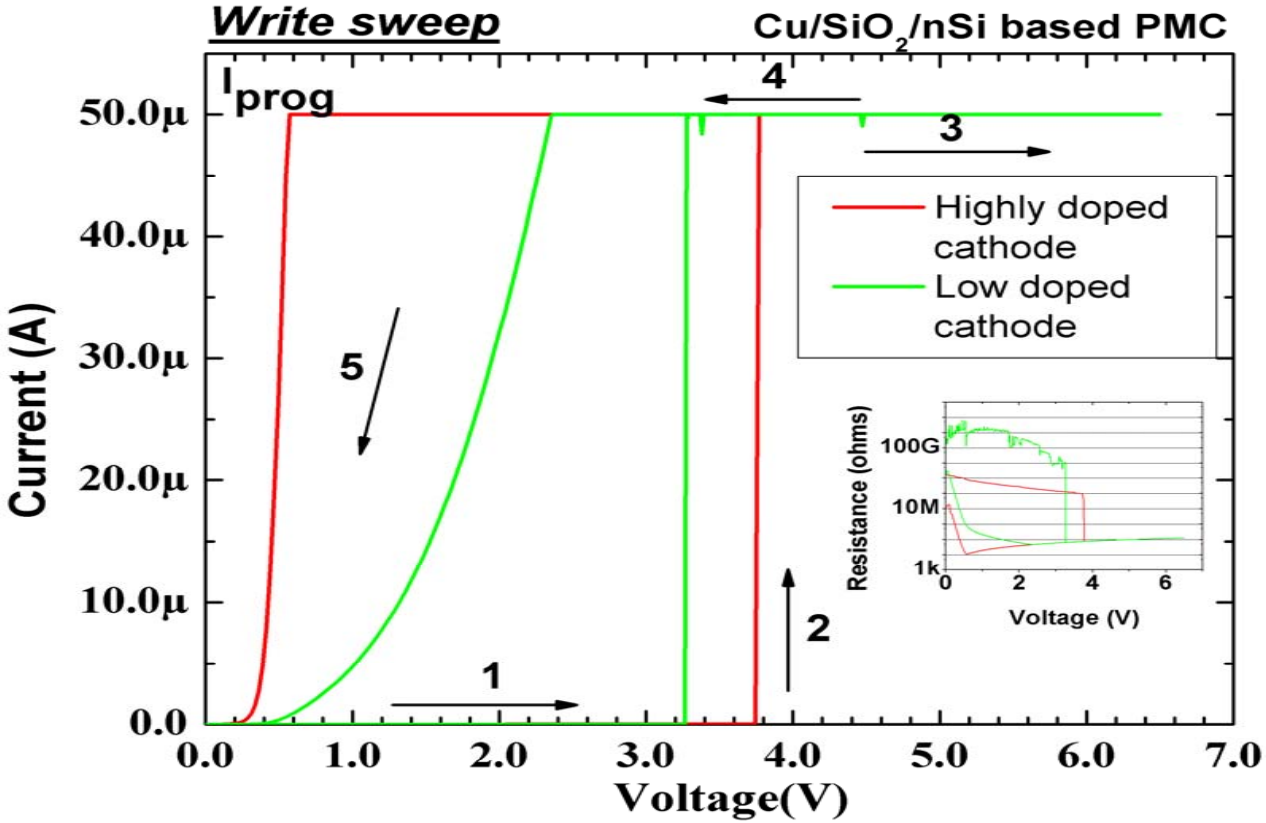


Cu top electrode - 35 nm

Cu doped SiO_2 - 15 nm

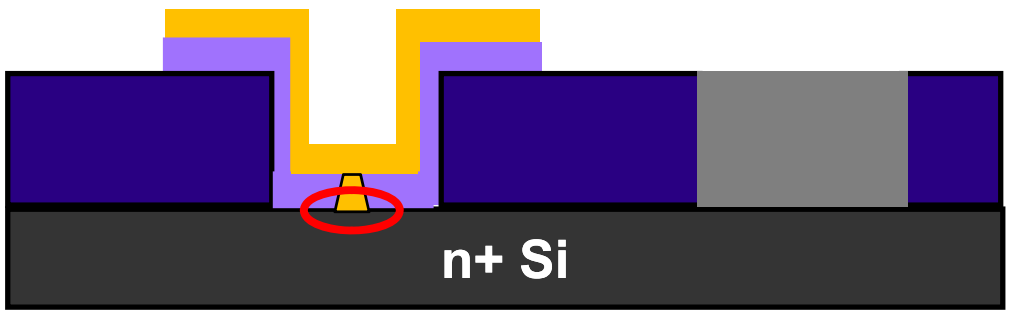
Al - 200 nm

Dielectric



Data from Sarath C. Puthen Thermadam, ASU

Integrated diode isolation - erase



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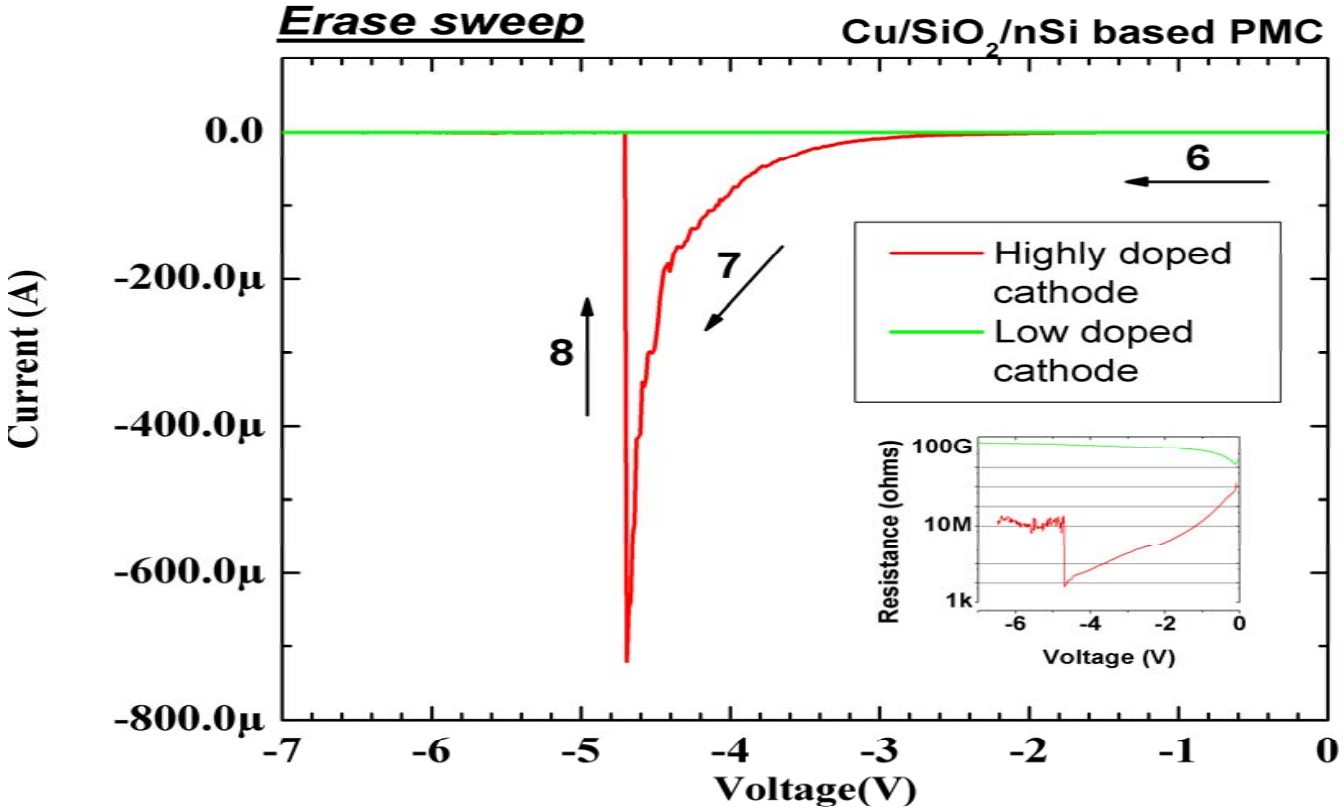

Data from Sarath C. Puthen Thermadam, ASU

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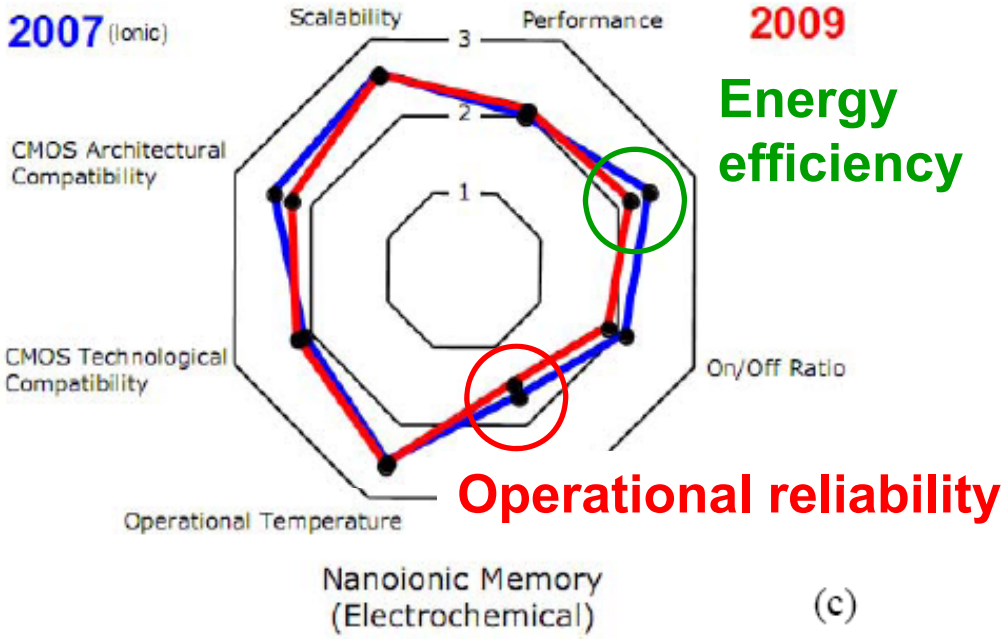
International Technology Roadmap for Semiconductors



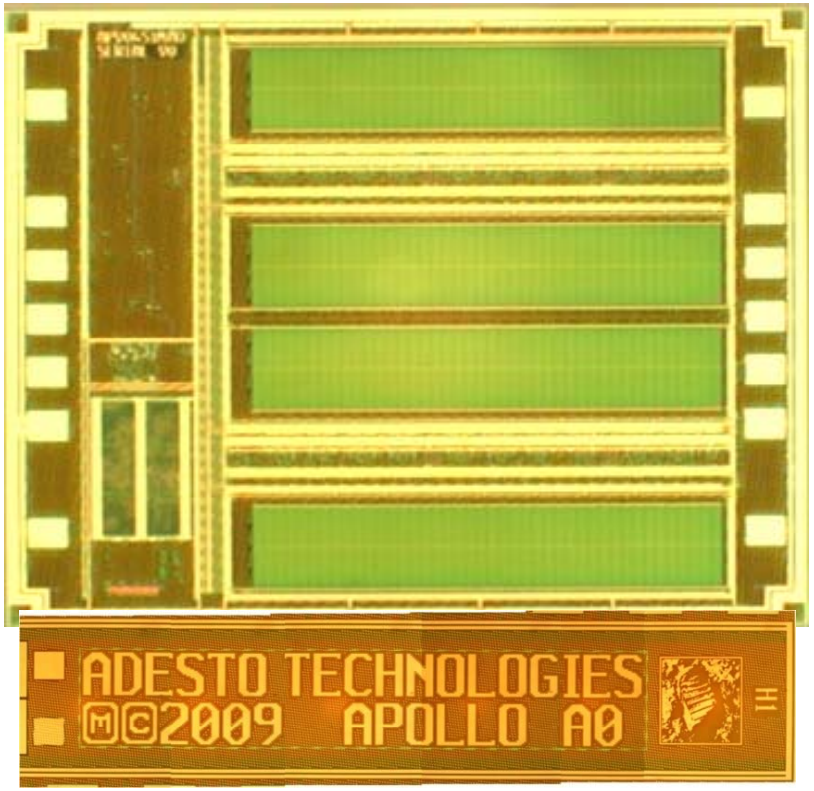
Energy efficiency

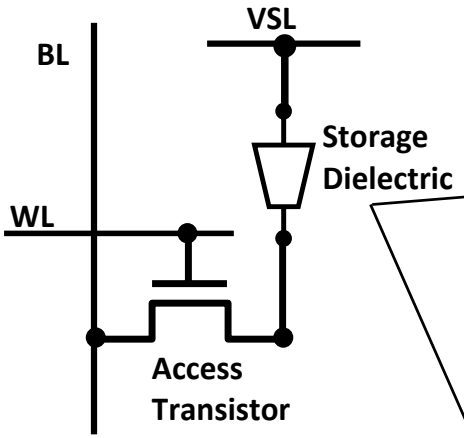
Operational reliability

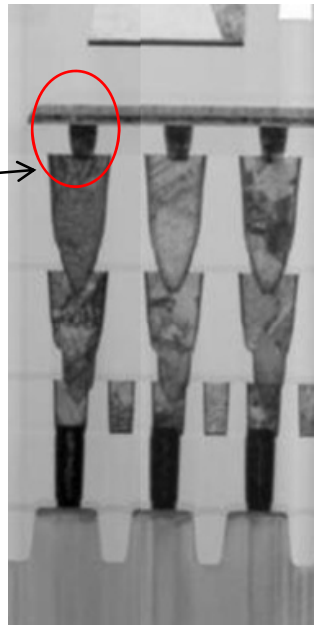
Ionic memory gained a formal place in the ITRS in the 2007 Edition

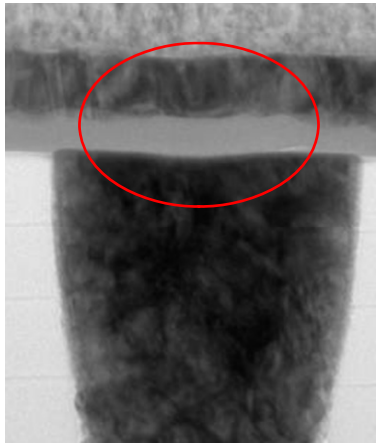
Operational reliability is still a concern for most RRAM contenders but energy efficiency looks promising for ionic memory

130nm (Cu BEOL) integration









Salient Features:

- 1Mb EEPROM/Flash Macro on Standard Foundry 130nm
- Programmable elements requires 2 non critical masks in BEOL flow
- Cell size determined by access device, core cell will scale with CMOS

It’s alive!

Image downloaded and stored on the hard drive

Image stored and read back on Adesto serial device

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Thank you for your attention!

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